The performance figures quoted are subject to normal manufacturing and service tolerances

The right is reserved to alter the equipment described in this manual in the light of future technical development.

WARNING

The Power Amplifier PWB uses semiconductors containing Beryllium Oxide. If inhaled, dust from this oxide can be toxic.

No danger can arise from normal handling but no attempt should be made to tamper with these devices.

They should not be discarded with industrial or domestic waste.

A full list of these devices is given in the Parts List.

VHF/UHF FM MOBILE RADIOTELEPHONE SERIES FM1000

SERVICE MANUAL
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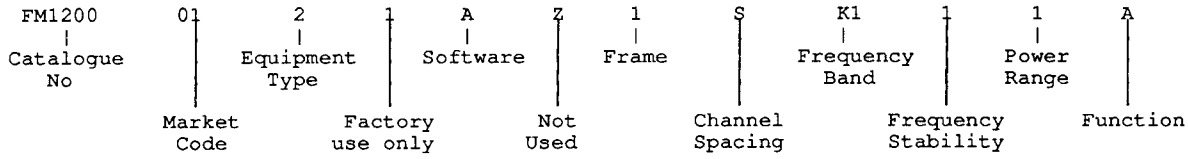
TP253

EQUIPMENT VARIATIONS

The sub-assemblies fitted to the transceiver will vary according to the role in which it is used. The complement of sub-assemblies for any particular equipment is indicated by an ordering code number marked on the equipment caseback. A typical order code number is given below, together with a list of codes which are not self-explanatory.



Market Code

01 Standard production
02 France
03 West Germany
09 Canada
12 Finland
19 Malaysia
30 Hong Kong

Equipment Type

2 FFSK Transceiver Type FM1200
3 FFSK Transceiver Type FM1300

Software

0 Less EEPROM and EPROM
A FM1200, Standard Console
B FM1200, Keypad Console
C FM1300, Standard Console
D FM1300, Keypad Console

Frame

1 Standard Frame
2 Extended Frame (required for Keypad Console and/or External MODEM)

Channel Spacing

S 12,5kHz
R 20kHz
V 25kHz

Frequency Band

E0 68 - 88MHz
B0 132 - 156MHz
A9 146 - 174MHz

K1 174 - 208MHz
K2 192 - 225MHz

TM 400 - 440MHz
T4 425 - 450MHz
U0 440 - 470MHz
W1 470 - 500MHz
W4 500 - 520MHz

Frequency Stability

1 ±5ppm
2 ±2ppm

Power Range

1 Standard VHF (1-25/30W)
2 Standard UHF (6-25W)
3 Low Power UHF (1-6W)

Function

0 Less Control/Digital-Signalling PWB
A FM1200 (FM)
B FM1200 with Modem Interface (FM)
C FM1300 (FM)
D FM1300 with Modem Interface (FM)
E FM1200 (PM)
F FM1200 with MODEM Interface (PM)
G FM1300 (PM)
H FM1300 with MODEM Interface (PM)

SECTION 1
GENERAL INFORMATION

SUMMARY OF DATA

General

Operation	Single or two frequency simplex.
Modulation	Phase (F3E).
Frequency Bands	E0 68 - 88MHz B0 132 - 156MHz A9 146 - 174MHz K1 174 - 208MHz K2 192 - 225MHz TM 400 - 440MHz T4 425 - 450MHz U0 440 - 470MHz W1 470 - 500MHz W4 500 - 520MHz
Channel Spacing	12,5kHz (type S), 20kHz (type R) or 25kHz (type V)
No of Channels	Up to 100
Power Supply	12V (nominal) DC vehicle battery, negative earth.
Antenna Impedance	50Ω
Maximum Current	Transmit: <7,0A Receive: <1,2A Standby: <700mA
Switching Bandwidth	Complete frequency band on receive and transmit.
Temperature Range	Operation: -30°C to +60°C ambient. Storage: -40°C to +85°C ambient.
Crystal Stability	Standard: ±5,0ppm Option: ±2,0ppm
Cabinet Radiation	To CEPT or relevant national specification.
Weatherproofing	Water and dust resistant to IEC529.

Dimensions	**Local Mount**	**Remote Mount**
Transceiver with cradle:	Height: 39mm + 17mm "chin" Width: 185mm Depth: 210mm (transceiver requires at least 260mm depth to clear rear connectors and cables).	39mm 185mm 210mm
Junction Box:	60mm x 53mm x 27mm (less cables & connector)	
Display Console:	143mm x 57mm x 30mm	
Loudspeaker (standard):	135mm width, 105mm height, 63mm depth, excluding bracket.	

Weight	Transceiver Unit:	1,6kg
	Console:	0,16kg
	Loudspeaker (Standard):	0,6kg
	(Compact):	0,19kg
Construction and Finish	Die-cast aluminium frame and pressed aluminium (sheet) covers. Textured paint finish.	

Transmitter

Power Output Range	1 to 30W: 68MHz - 88MHz, 132MHz - 174MHz 1 to 25W: 174MHz - 225MHz 1 to 6W: 400MHz - 520MHz (Low Power) 1 to 25W: 400MHz - 520MHz (High Power)
Standard Power levels	1W, 6W, 10W, 15W, 25W, 30W (output power software programmable per channel).
Spurious and Harmonics	<0,2µW between 0 - 1GHz.
Hum and Noise	To CEPT or relevant national specification.
Modulation Response	6dB/octave (+1dB/-3dB) pre-emphasis characteristic between 300Hz and 3000Hz (2550Hz 12,5kHz systems). Response may be altered to comply with local regulatory requirements.
Modulation Distortion	Less than 2% (at 60% peak system deviation with 1kHz modulation)

Receiver

Reference Sensitivity	12dB SINAD for 0,31µ230V (PD) signal input modulated by 1kHz tone at 60% peak system deviation.
Intermediate Frequencies	21,4MHz and 455kHz
Adjacent Channel Selectivity	Greater than 70dB.
Audio Output	3W RMS minimum into 3Ω load at less than 5% distortion. (1,5W as measured in accordance with CEPT TR24.01 Annex II recommendations). Receiver audio output is reduced to 0,5W RMS (±0,2W) when using the 50 metre Control Cable Kit."
Audio Response	6dB/octave (+1dB/-3dB) de-emphasis characteristic between 300Hz and 3kHz.

Tone-Signalling

Address Code Form (SELCALL)	Between 4 and 17 sequential tones.	
Tone Frequency Range	SELCALL:	810 - 2800Hz (see Table 1.1 for specific frequencies).
	CTCSS:	67,0 - 250,3Hz (see Table 1.3 for specific frequencies).
	FREE TONE:	563Hz, 600Hz, 638Hz, 679Hz, 723Hz, 770Hz, 820Hz, 873Hz (Decode only).
Link Establishment Time (LET)	10ms - 2,55s (in 10ms increments)	
Inter-FreeTone Period	0 - 25,5 seconds (in 100ms increments).	

TABLE 1.1 - SELCALL TONE FREQUENCIES (All frequencies in Hz)

FUNCTION	CODING CHARACTER	SYSTEM TONE FREQUENCIES							
		Philips ST-500							
		CCIR/EEA Type 1	ZVEI Type 2	DZVEI Type 3	CCIR Type 4	EEA Type 5	ZVEI Type 6	DZVEI Type 7	ZVEI2 Type 8
"0" TONE	0	1981	2400	2200	1981	1981	2400	2200	2400
"1" TONE	1	1124	1060	970	1124	1124	1060	970	1060
"2" TONE	2	1197	1160	1060	1197	1197	1160	1060	1160
"3" TONE	3	1275	1270	1160	1275	1275	1270	1160	1270
"4" TONE	4	1358	1400	1270	1358	1358	1400	1270	1400
"5" TONE	5	1446	1530	1400	1446	1446	1530	1400	1530
"6" TONE	6	1540	1670	1530	1540	1540	1670	1530	1670
"7" TONE	7	1640	1830	1670	1640	1640	1830	1670	1830
"8" TONE	8	1747	2000	1830	1747	1747	2000	1830	2000
"9" TONE	9	1860	2200	2000	1860	1860	2200	2000	2200
GROUP TONE	A	1055	970	825	2400	1055	2800	2600	886
EXTENDED TONE	B	—	—	—	930	930	810	—	—
ALARM TONE	C	2400	2800	2600	2247	2247	970	886	810
SELECTABLE TONE	D	—	—	—	991	991	886	810	—
REPEAT TONE	E	2110	2600	2400	2110	2110	2600	2400	970

Note: ***The number of tones sent will normally be dictated by the system the equipment is to be used with.***

Not all combinations of frequency bands, options etc are available for every market area.

TABLE 1.2 - TONE LENGTH AND CALL DURATION

SIGNALLING SYSTEM	TONE LENGTH
CCIR (Philips ST-500)	100ms
EEA (Philips ST-500)	40ms
ZVEI (Philips ST-500)	70ms
DZVEI (Philips ST-500)	70ms
CCIR (Tone Type 4)	100ms
EEA (Tone Type 5)	40ms
ZVEI (Tone Type 6)	70ms
DZVEI (Tone Type 7)	70ms
ZVEI2 (Tone Type 8)	70ms

TABLE 1.3 - CTCSS TONE FREQUENCIES

No	Freq	No	Freq	No	Freq	No	Freq	No	Freq	No	Freq
1	67,0	8	88,5	15	110,9	22	141,3	29	179,9	36	233,6
2	71,9	9	91,5	16	114,8	23	146,2	30	186,2	37	241,8
3	74,4	10	94,8	17	118,8	24	151,4	31	192,8	38	250,3
4	77,0	11	97,4	18	123,0	25	156,7	32	203,5		
5	79,7	12	100,0	19	127,3	26	162,2	33	210,7		
6	82,5	13	103,5	20	131,8	27	167,9	34	218,1		
7	85,4	14	107,2	21	136,5	28	173,8	35	225,7		

TABLE 1.4 - DTMF FREQUENCIES (DTMF microphone only)

Tone Frequency Pairing		High Frequency Group (Hz)		
		1209	1336	1477
Low Frequency Group (Hz)	697	1	2	3
	770	4	5	6
	852	7	8	9
	941	*	0	#

FREQUENCY TRIMMING

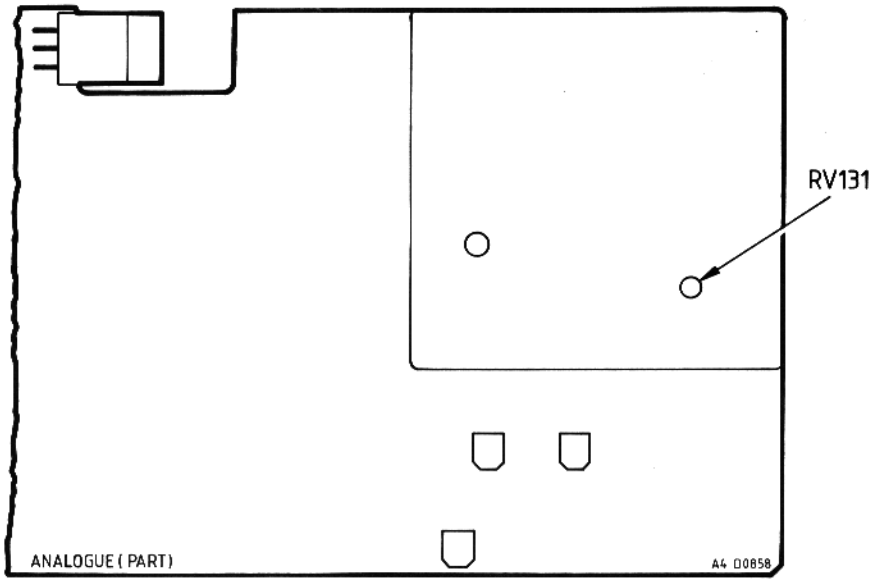
The reference oscillator in all FM1000 series radios is preset before leaving the factory and should not require further adjustment. An oscillator that has drifted out-of-calibration may be the cause of distorted reception and, in extreme cases only, no reception at all.

If it is suspected that the reference oscillator is out-of-calibration, it may be reset as detailed in the Service Manual. A frequency counter that is known to be accurate is required. If in doubt, return the radio to your dealer.

Note that in synthesised equipments such as the FM1000 series radio, all receive and transmit channel frequencies are derived from one crystal-controlled reference oscillator. It is not possible to 'net' channels on an individual basis, and therefore, it is imperative in radio systems incorporating such equipments that base station transmitters and receivers are tuned exactly to their allocated frequencies.

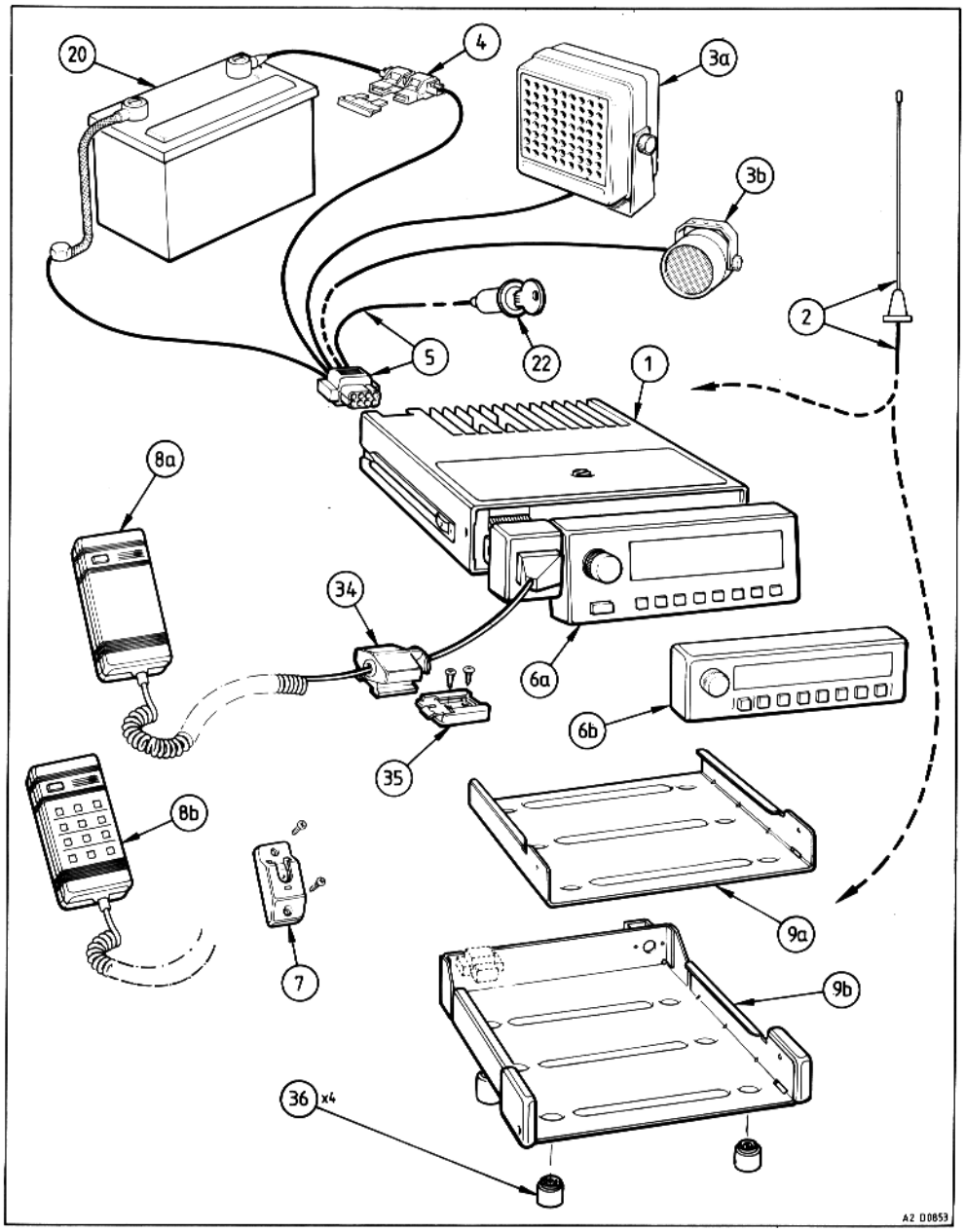
Note: The frequency counter used for frequency trimming must be known to be in calibration or have recently been checked against a reliable frequency standard. Always allow a frequency counter to warm-up prior to use.

1. Connect loudspeaker and microphone to the radio.
2. Connect the power supply to the radio, ensuring that the positive lead is fused and that supply polarity is correct (negative ground). Adjust the power supply to 13,2V DC.
3. Connect RF power meter and set to the appropriate range (50W for high power radios). Connect a frequency counter to the meter via a 20dB attenuator.
4. Remove the large cover from the radio.
5. Switch on the radio and allow a five-minute warming-up period to elapse.



Location of RV131

6. Operate the press-to-talk switch and adjust RV131 on the Analogue PWB to set the frequency counter to the EXACT frequency of the selected channel.
7. Switch off radio, disconnect test equipment and refit cover to radio.



Basic Installation Diagram for Local Control

The item reference numbers apply to the installation procedures only:

(1)	Radio	(15)	Fascia (for Remote Control)
(2)	Antenna and Feeder Cable	(16)	Console Plate
(3a)	Loudspeaker, standard	(17)	9-way Connector
(3b)	Loudspeaker, small	(18)	Magnet
(4)	Fuseholder	(19)	Key (Cradle release)
(5)	Battery Lead Assembly	(20)	Vehicle Battery
(6a)	Standard (4-6 digit) Console	(21)	Console Cable (9-way)
(6b)	Basic Console	(22)	Vehicle Ignition Switch
(7)	Rest (Mic Installation Kit)	(23)	Volume Control Knob
(8a)	Microphone, standard	(24)	Front Panel, Console
(8b)	Microphone, DTMF	(25)	Rear Panel & PWB, Console
(9a)	Cradle, standard mount	(26)	Graphics Panel
(9b)	Cradle, Cassette mount	(27)	Bezel
(10)	Junction Box	(28)	Scotchlok Connector
(11)	Control Cable, 1, 5 or 50m	(34)	Strain Relief Clamp
(12)	Mate n' Lock Housing	(35)	Clamp Support
(13)	Bracket, Console	(36)	Spacer, Cradle (4 off)
(14)	Cradle, Console		

Note: The 50-metre control cable is unsuitable for use with Basic Consoles, DTMF and Keypad microphones.

SECTION 3
TECHNICAL DESCRIPTION

CIRCUIT SUMMARY

The transceiver consists of five PWB assemblies as in FM1100, but the Control PWB is replaced by the following assembly:-

DIGITAL SIGNALLING	comprising Non-Prescribed Data PWB (optional), main transceiver microprocessor with clock oscillator, EPROM, EEPROM, RAM, Shift Registers, timers, 30V generator and FFSK signalling circuits comprising microprocessor, EPROM, Address Latch, RAM, MODEM and peripheral devices.

All FM1200 control and signalling functions are provided by the Control/Digital Signalling PWB assembly. This PWB contains two 80C31 microprocessors IC312,IC548. IC312 acts as the main control for the FM1200, and communicates with peripheral devices (eg consoles and data programmers) via a serial bus. The bus is interrogated on a regular basis and the state of the FM1200 altered depending on information received. Control of the analogue part of the radio is achieved via serially driven shift registers, the outputs of which directly control the analogue functions. Certain internal voltages within the FM1200 radio are monitored via an Analogue-to-Digital (A-to-D) converter (IC301) and an input shift register (IC303). Customisation data, such as the frequency band and the key and indicator functions, are held in EEPROM (IC311) to which the microprocessor has access. IC548 controls all 'over the air' signalling via an FFSK MODEM (IC546). It decodes the incoming bit stream from the MODEM to detect valid signalling. Relevant signalling messages are then passed via a dedicated serial bus to the control microprocessor (IC312). Encoding of FFSK for transmission is performed by the signalling microprocessor which outputs binary data to the MODEM which converts it into FFSK audio.

The Non-Prescribed Data PWB allows interface between the radio and an externally-mounted MODEM. Sequential tone information generated by the signalling microprocessor may be processed on this PWB prior to transmission by the radio.

CONTROL/DIGITAL SIGNALLING PWB

Power Supply Circuits

When the FM1200 radio is switched on, unregulated DC is supplied to the Control PWB from the Analogue PWB via SKTB. This is used to supply two single chip voltage regulators which provide outputs of 5V and 8V respectively. The 5V line is used to feed the logic control circuitry and 8V is used to supply the audio circuitry for the FFSK signalling.

The unregulated DC input is also used to supply the 30V generator circuit which is required for the synthesiser loop filter. This is generated by IC318, a charge pump device. Adjustment of the 30V output is achieved by RV301 which senses the rectified and smoothed output of the device and feeds it back to its control pin.

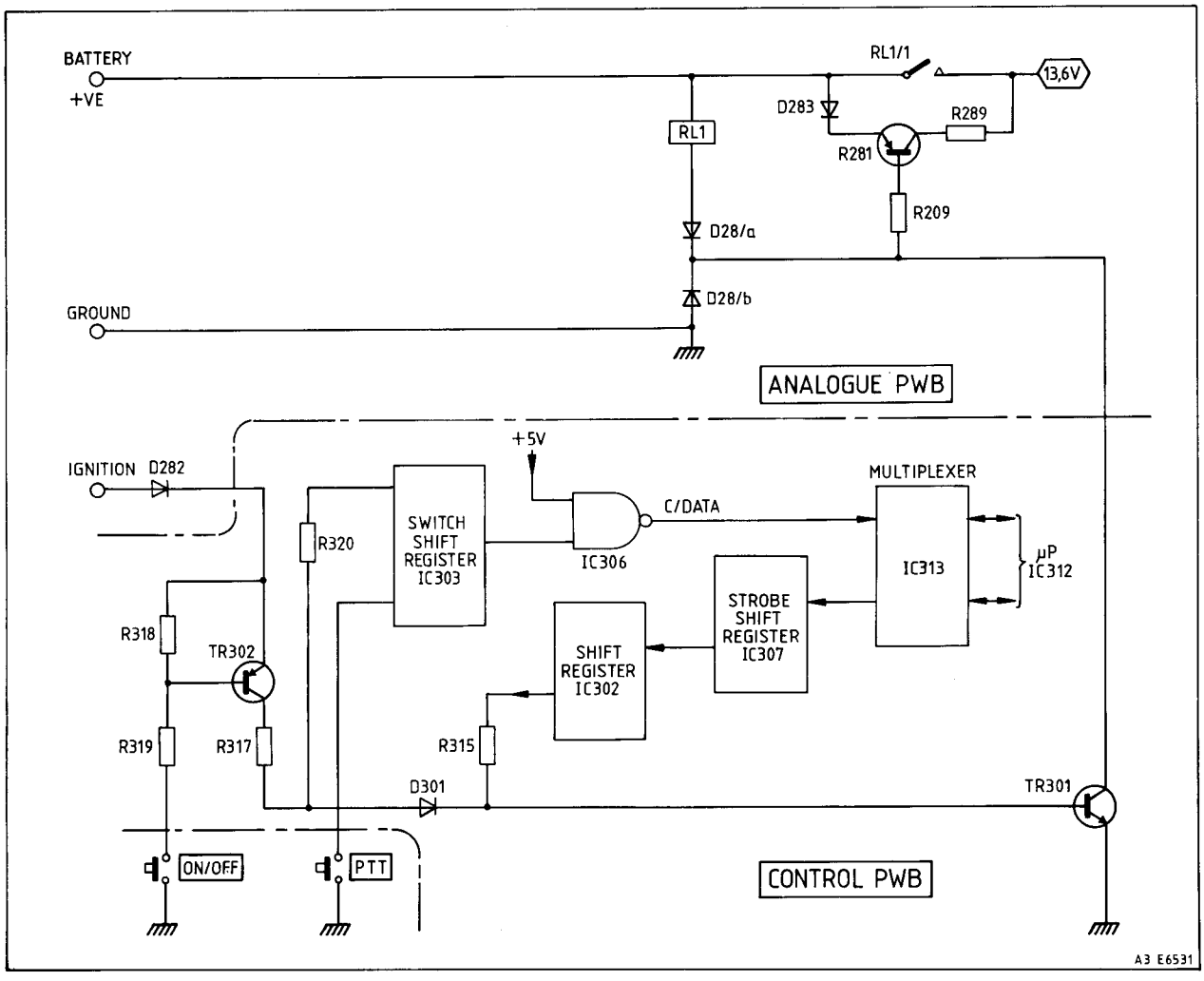


Fig 3.1 Power Supply Circuits Block Diagram

ON/OFF CIRCUIT

DC power from the vehicle battery (or other external PSU) is switched on or off by a relay mounted on the Analogue PWB. To switch the equipment on, the Ignition line must be connected to the external DC supply and the incoming on/off control line grounded (eg: by pressing the console on/off switch or plugging in a data programmer). TR302 effectively forms an AND gate with the ignition and on/off inputs. When the ignition line (TR302 emitter) is high and on/off line (TR302 base resistor) is low, TR302 switches on. This in turn switches on TR301, the collector load of which is the power on/off relay. When this occurs, the control microprocessor can hold the FM1200 radio on by setting Q4 of IC302 high. This feature also enables the data to be saved to EEPROM after detecting switch off. The state of the on/off line is monitored via the D0 input of the switch input register IC303.

CONTROL MICROPROCESSOR

The control processor uses a nominal 12MHz clock frequency. This is provided by TR307, TR306, TR305 and XL301 which form a pullable oscillator circuit. On power up the microprocessor requires to be reset. This is performed by IC314 which applies a positive pulse of approx 20ms at the reset input of the microprocessor when it detects the 5V supply rail ramping up. In normal operation no further reset pulses should be applied.

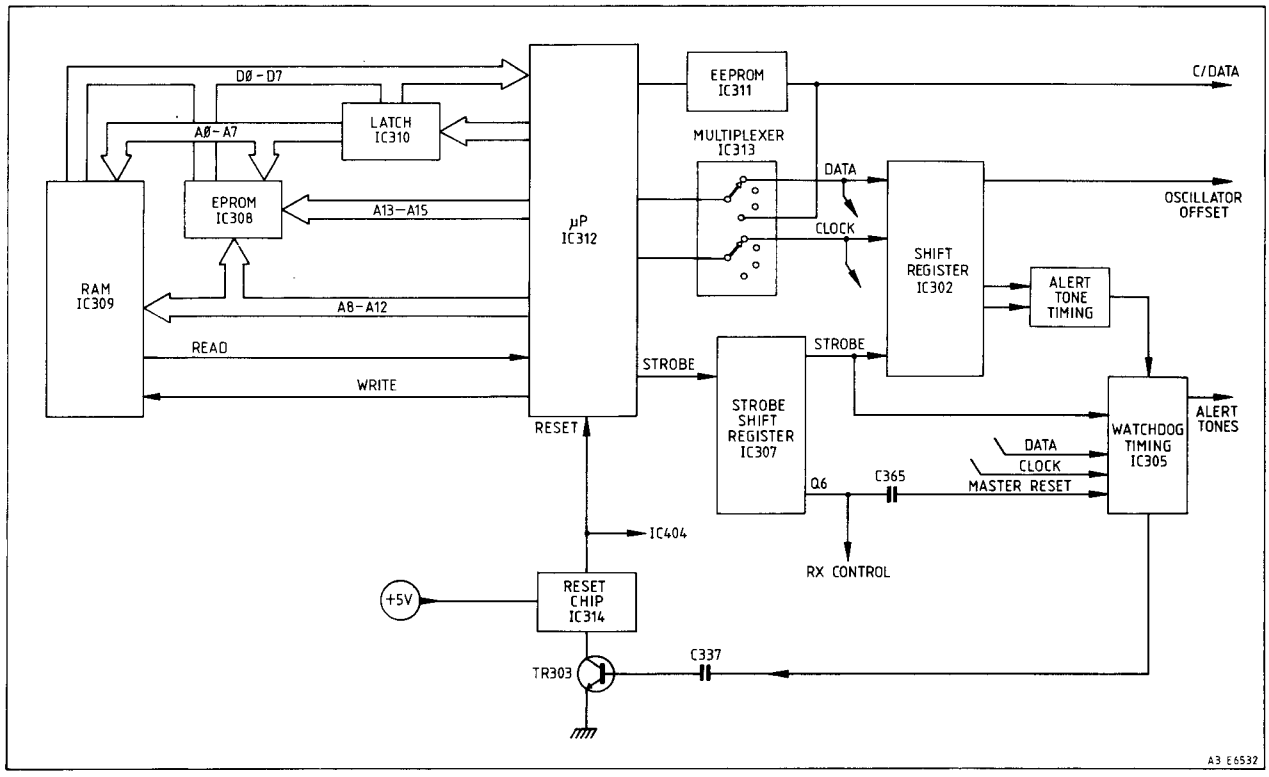


Fig 3.2 Microprocessor Block Diagram

The microprocessor executes software code held in a 64K EPROM (IC308) which it accesses via its external address/data bus D0 to D7 and A8 to A15. The device operates on a 8-bit wide data bus and 16-bit address bus. In order to reduce the pin count of the 80C31, the low order address bus is multiplexed with the data bus. To separate these functions an address latch (IC310) is used. This acts as a transparent latch gated by its LE input. When the microprocessor outputs its low order address it also sends out a positive pulse on its ALE line which gates the low address through to the output of the latch. Also connected to the external bus is an 8k x 8 static RAM (IC309) which also uses the address latch, but control of Read and Write functions is via two separate control lines from the microprocessor, "/RD" and "/WR".

To avoid data corruption during short power interruptions (FM1200 only), the RAM supply voltage is fed via a series diode and reservoir capacitor, which can maintain the contents of the RAM for at least 20 seconds. To avoid corruption at reset the reset pulse is inverted by TR309 which sets CHIP SELECT 'low', disabling the RAM for the duration of the reset pulse.

When first switched on, the microprocessor software will initialize the FM1200 radio by commands sent on the serial bus. Ports 3.1 and 3.0 on IC312 connect to a serial UART held on chip. This can be configured in a number of different ways determined by the radio software. The FM1200 utilizes two of the available UART modes and further sub-divides these depending on whether the bus connects to an external device or devices internal to the radio. A bi-directional multiplexer IC312 is used to connect the serial UART to each bus in turn. Selection is controlled by P1.1 and P1.0 of the microprocessor. The operation of each bus is explained below:

INTERNAL EXPANSION BUS (IEB)

This bus is formed by lines CLK and C/DATA from pins 11 and 4 of the multiplexer IC313. It is used to drive a number of Input and Output shift registers contained on both the Control PWB and the Analogue PWB.

To write to an output shift register (74HC4094), the microprocessor writes data into the shift registers on the C/DATA line. The Clock signal is provided by the CLK line which is connected to all shift registers on this bus. To write to any of the shift registers, it first sends out an 8-bit data byte corresponding to the output pattern it wishes to write to the selected shift register. This data will be stored in the strobe shift register (IC307). This is immediately followed by an address byte for the selected shift register. As the address byte is clocked into the strobe shift register the previous data byte is clocked out of it (on pin 10) and is clocked via the data inputs into all the output shift registers on the bus. By applying a pulse on P1.4, the strobe and output enable of IC307 are momentarily enabled causing, the address byte to appear on its parallel outputs. This byte will be chosen so that a '1' is passed to the strobe of the required output register, hence only that shift register will be strobed, latching the required data byte onto its parallel outputs.

To read from the switch input shift register (74HC165), a similar technique is used. Bit Q4 of the strobe shift register is sent momentarily low. This is connected to the shift load input of the Switch Input Register IC303, causing data on its parallel inputs to be loaded into IC303's internal shift register. By applying eight clock pulses on the CLK line the data is serially clocked out from IC303 pin 9 via an open collector NAND gate (IC306) and read in by the microprocessor. To avoid contention when writing to the C/DATA line from the microprocessor, the open collector output of this NAND gate must be set high. This is achieved by sending eight clock pulses to the switch input register (which has its serial input tied to 0V), thus filling the shift register with '0's.

The switch input register is read every 10ms. Output devices on this bus are written to as required.

EXTERNAL EXPANSION BUS (EEB)

This bus operates in an identical manner to the Internal Expansion Bus but uses separate CLK, C/DATA and Strobe lines. It is used to interface with certain ancillaries such as the Keypad Microphone which has internal shift registers in it. Each ancillary also contains a separate strobe shift register which is enabled by a strobe signal from P1.2 of the microprocessor. IC315 is used as a line driver. When writing out on the bus the microprocessor enables this line driver by switching P1.3 low. Taking P1.3 low also sets the output of a NAND gate in IC306 high during writing to avoid bus contention. When P1.3 is set high the microprocessor reads from the bus. Incoming data is buffered by IC315 and passed via IC306 (now enabled) and IC313 to microprocessor IC312.

When first switched on, the microprocessor will read the bus to detect if any ancillary is connected. If so, it will 'poll' the bus every 10ms; otherwise the bus will be ignored until the FM1200 radio is next switched on or is reset.

EXTERNAL MESSAGE BUS (EMB)

In this mode the UART is set up as a 378 kilobit serial link communicating on the TxD and RxD lines on SKTC/PLA. The EMB is used to communicate with complex peripherals such as the Standard Console or the Portable Data Programmer. At switch-on, IC312 sends out a series of pre-defined messages to all the possible peripherals which can be connected to the radio. If connected, the peripheral will respond to the message and IC312 will then send out messages to the device every 10ms. If a peripheral device is not connected at the time of switch on, and hence doesn't reply, IC312 will assume that it is not connected and send no more messages to that device.

INTERNAL MESSAGE BUS (IMB)

This bus is similar to the EMB. However, the signalling microprocessor is the only device connected to it. To ensure fast communication from the signalling microprocessor to the control microprocessor, use is made of the control micro's INT0 input (to avoid having to wait for the control micro to request the transaction).

Analogue-to-Digital (A-to-D) Converter

IC301 is an 8-bit resolution A-to-D converter. It is used for monitoring the state of various voltages from the RF and audio parts of the radio. The following inputs are used:

1 Tune Volts:	This is used for monitoring the VCO tuning voltage. If it is outside a certain range, it will increment a hardware error count in EEPROM. The radio will, however, remain operational.
2 Supply voltage:	This is used when monitoring transmitter power to detect whether a reduction in transmitter power was caused by a reduced supply voltage.
3 Tx Temp:	This is connected to a thermistor circuit held in the transceiver casting. If an excessive temperature is detected, the control unit will reduce the transmitter power by steps until the temperature falls again, or zero power is reached. If zero power is reached, the FM1200 radio will switch back to receive mode.
4 Noise Level:	This is used to determine the quieting of the receiver and, if appropriate, open the squelch.
5 RSSI:	This is a DC signal from the IF amplifier, used to determine the signal strength. It is used for squelch control and when hunting for a suitable channel to communicate with the trunked radio network.
6 Power Level:	This input is from a diode detector circuit on the PA. It is used to monitor the transmit power. If excessive or too little power is detected, the output power is reduced in steps in the same way as with excessive temperature.
7 Volume:	This input comes from the console volume potentiometer which gives a DC level depending on its setting. The microprocessor sets the digital audio attenuator on the analogue board according to this value.
8 Hook/Facility Switch:	This is an input from the microphone. These switches are connected with resistors in such a way that the voltage on this pin depends on which combination of switches are closed, and enables their operation to be detected by the microprocessor software.

The A-to-D convertor uses the 5V rail on the Control PWB as a reference. It is driven from the Internal Expansion Bus using a method similar to that employed for the input and output shift registers. To enable a conversion, the microprocessor uses the IEB to inform the device which of the inputs is required to be converted. It then takes P3.5 low to signal that conversion should now take place. The chip uses the ALE line from the microprocessor as its system clock. (On average ALE will run at 2MHz as code is executed from the EPROM.)

Alert Tone Generator/Watchdog Timer

The alert tone generator is a simple RC inverter oscillator made up of C326,R328 to R331 and IC305 which contains on-chip inverters. The alert tone frequency and gating is controlled by IC302. The shift register outputs of IC302 are used to modify the oscillator's RC time constant depending on which alert tone is required, and the Q7 output is used to gate these tones on or off. The resultant audio is mixed with the loudspeaker audio on the Analogue PWB. IC305 also contains a series of cascaded dividers which reduce the RC oscillator frequency down by factors of 2. If allowed to run for long enough, a pulse will appear on the divider output at pin 1, causing TR303 to switch on and the reset chip to send a pulse to reset the microprocessors. In practice, this is prevented by C365, which transmits pulses from the strobe shift register and resets the cascaded dividers within IC305. However, if the software is not running properly, this will not occur, and a reset pulse will be generated.

Microprocessor Oscillator

IC312 is supplied directly from the oscillator output and supplies the signalling microprocessor via an internal buffer from its XTAL2 output. XL301, TR305 and associated components form a standard Colpitts oscillator. Transistors TR306, TR307 are used to switch in a different crystal load capacitance depending on the logic level at Q1 of IC302. The oscillator frequency can thus be offset slightly when a direct harmonic of the crystal falls close to the current receive frequency. Each time the radio tunes to a new channel, the microprocessor calculates whether frequency offset is necessary, or not. When transmitting, the oscillator is always set to its nominal 12,096MHz.

EEPROM

IC311 is a serial EEPROM used for storage of all customisation data. Depending on customer requirements a 512 byte or 2 kilobyte device is fitted (X2404 and X24C16 respectively). Electrical operation with each device is similar. On power up, the FM1200 radio reads customisation data into RAM before normal operation is commenced. The device uses I^2C protocol which utilizes a CLK and DATA line to communicate with the microprocessor. When the microprocessor is communicating with this device, it uses the C/DATA line on the IEB to send and receive data, but generates a separate clock output from P1.5.

If any customisation data is modified (eg by a PDP), the microprocessor will save the changes to EEPROM at switch-off. If there are a substantial number of changes to the customisation data, there will be a noticeable delay between switching off at the console and the FM1200 internal relay opening (power down).

External Alert

This circuitry can be used as either an input or an output. In normal operation this is used as an output to switch an external device (eg a car horn) when the mobile is called. In this case, the microprocessor sets p1.6 high to switch on darlington pair TR308/TR304. The Darlington pair connect to the External Alert pin on the external power socket. This output is also sensed by the microprocessor via R324 and the switch input register. At switch-on, P1.6 is set low and hence TR304 collector floats high. If the External Alert pin is taken to 0V before switch-on, the microprocessor detects that it is being used as an input. This mechanism is used to place the FM1200 radio into test mode (see Section 4 of TP253).

FFSK Encoder/Decoder

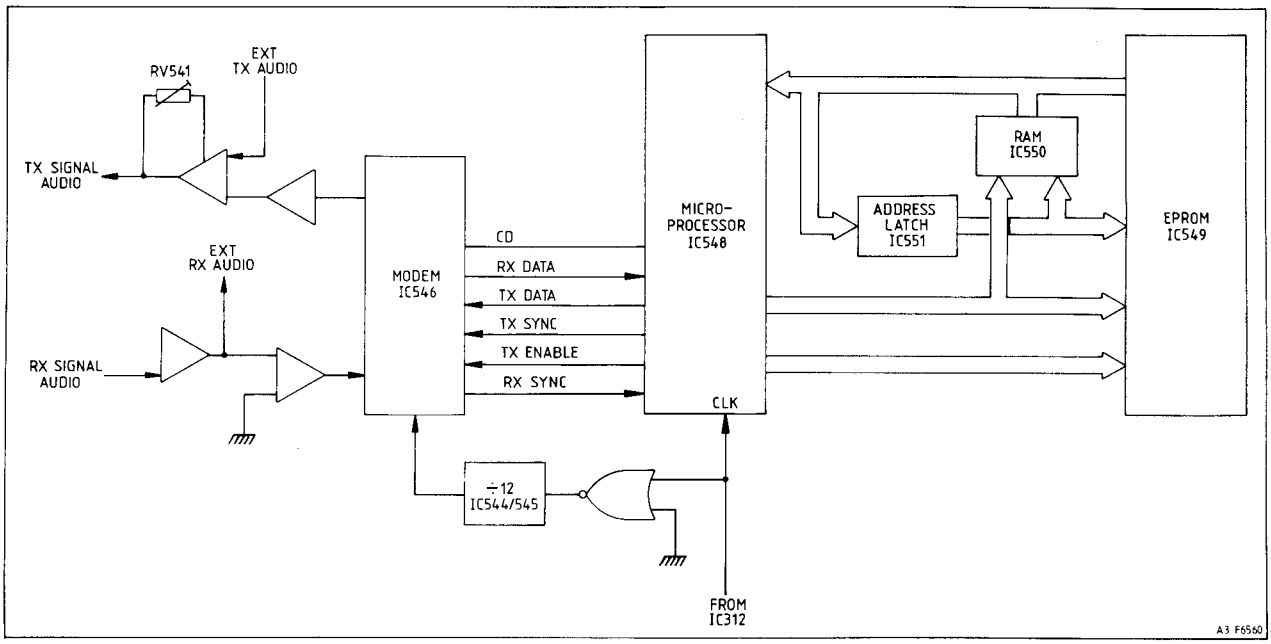


Fig 3.3 Digital Signalling Block Diagram

FFSK functions are controlled by microprocessor IC548 which relies on master processor IC312 for its clock signal (defining processing speed) and instructions from the console. Signalling data is stored in EPROM IC549, which is accessed via 8-bit address latch IC551. Data from the EPROM is loaded into RAM IC550 at switch on.

MODEM IC546 is a full duplex device, ie it can decode while encoding. Tx Data is clocked out from IC546 by pulses on the Tx Synch line from microprocessor IC548. Similarly, Rx Data is clocked in by Rx Synch pulses from IC548. A 1,008MHz clock signal is required to drive IC548; this is derived from IC312 clock. As IC312 clock runs at 12,096MHz, it is applied to flip-flops IC544, IC545, which divide the signal by 12 to produce 1,008MHz.

Signalling Microprocessor

The signalling microprocessor is also an 80C31 device and has external RAM (IC550) and EPROM (IC549) operating in a similar fashion to the main transceiver microprocessor. The signalling microprocessor interfaces with the FFSK MODEM IC546 via a number of control lines. The MODEM itself is a duplex device which is configured so that its receiver is permanently enabled. The transmit section generates 1800Hz and 1200Hz tones from incoming Tx Data sent to it at a bit rate of 1200bps. Tones and bit rate are generated by the MODEM from a reference frequency of 1,008MHz at its XTAL1 input. This is derived from the 12,096MHz microprocessor oscillator and divided by 12 by J-K flip-flops IC544 and IC545.

MODEM

CD - CARRIER DETECT

Carrier Detect is a logic signal sent from the MODEM receiver to the signalling microprocessor. A series of filters within the MODEM are set up to detect FFSK signalling frequencies. When FFSK signals are detected, the CD line goes 'high'. Operational speed of the CD line is determined by the value of C558 (connected to the CDT MODEM input) which controls a time constant within the IC.

RX DATA

This is the received serial data stream from the FFSK MODEM, which is read by the signalling microprocessor.

RX SYNC

This is a 1200Hz square-wave output from the MODEM, which is synchronised to the RxDATA output and is used to generate an interrupt to the microprocessor when the next bit of valid data is present on RxDATA. When no signalling or a noisy signalling is received, this output will exhibit 'jitter' as it repeatedly resynchronises.

TX EN - (TX ENABLE)

When the microprocessor wishes to transmit a message, it takes this line 'low' to enable the FFSK transmitter.

TX SYNC

This output is a 1200Hz square-wave from the MODEM. It is used to interrupt the signalling microprocessor to signal that it should output the next bit of data to be encoded. It will only be active when the TxEN is 'low'.

TX DATA

This line is used by the signalling microprocessor to output the data stream to be converted by the MODEM to FFSK audio.

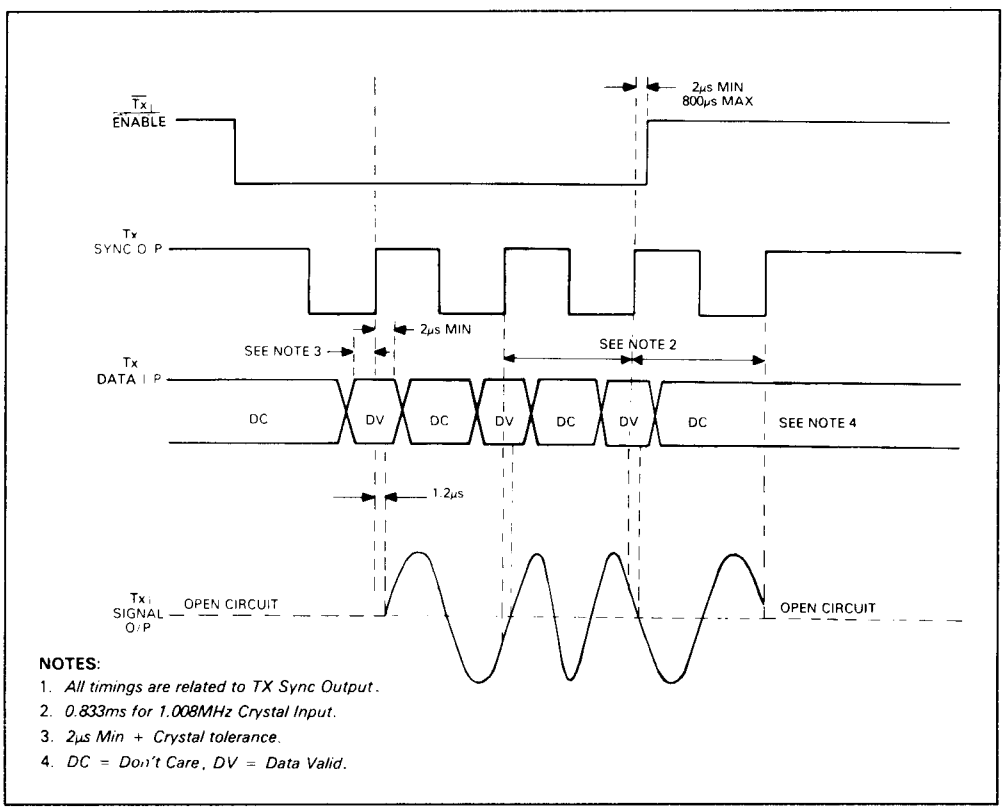


Fig 3.4 FFSK Transmit Timing Diagram

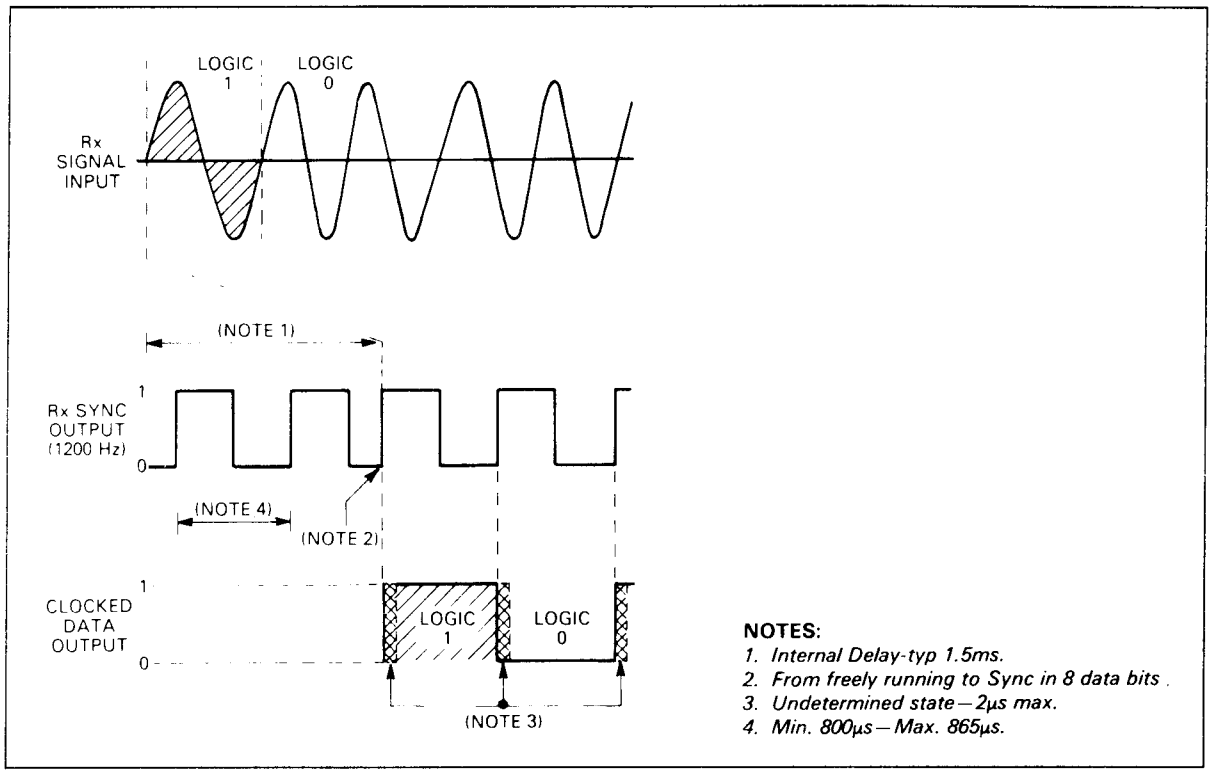


Fig 3.5 FFSK Receive Timing Diagram

FFSK Analogue Circuitry

FFSK is outputted from the Tx Audio output of IC546 when outgoing signalling is in progress. This signal is taken to inverting operational amplifier IC543, the gain of which is set via RV541 and associated resistors. The gain of this stage is altered to control the AF level to the FM modulator and hence set the required frequency deviation for data signalling. The bias pin from the MODEM is used to create a half rail for the operational amplifiers and is buffered by a unity gain amplifier (IC541). This output is fed through a low pass filter with a break point of approximately 15kHz to remove any high frequency components from the waveform. It is then fed to the modulator on the Analogue PWB.

Unfiltered receiver audio is fed (without filtering) from the Analogue PWB. It is buffered by part of IC541 and fed to a clipper amplifier (IC541) which uses a pair of back-to-back diodes and feedback network to supply the correct level of clipped audio signal to the MODEM. It is then buffered and presented to the MODEM via a unity gain operational amplifier. A separate half rail is provided for the receive circuit by R544, R545 and C546.

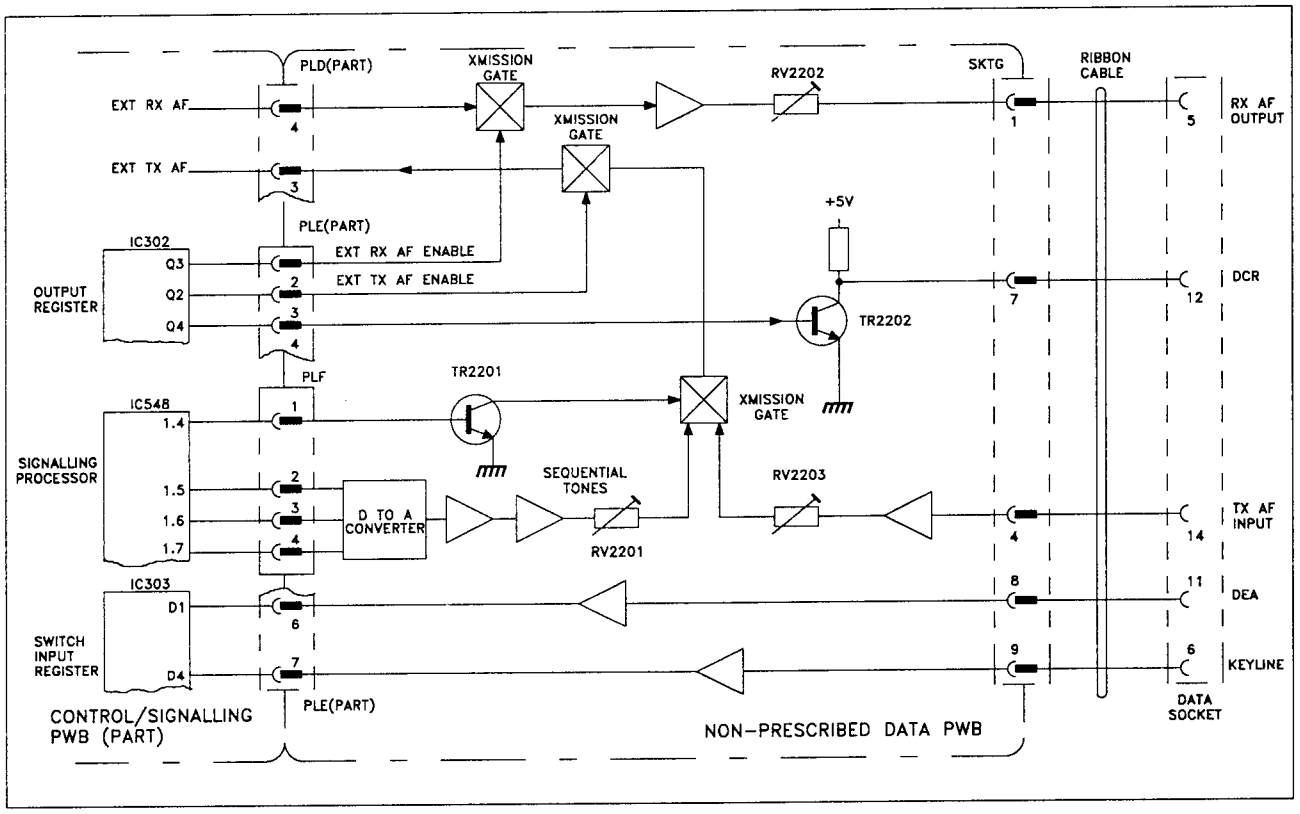


Fig 3.6 Non-Prescribed Data PWB Block Diagram

MODEM Interface

Unfiltered receiver audio at PLD4 is gated by IC204 which is enabled by the External Audio enable input, and then amplified by buffer IC205 to a 600ohm output on the front panel data socket. The gain of this section is adjusted by RV2202. Transmit audio from the external MODEM is applied via SKTG4 to IC2205 and is gain adjusted by RV2203. It passes two switches, the first, controlled by the signalling processor (Port 1.4), switches between external MODEM input and the on-board sequential tone encoder. This switch is set by default to enable transmission of data from the external MODEM, execpt when sequential tones are being generated. The second switch mutes audio to the Control PWB and is controlled by the Tx Audio Enable line. This switch is open except when accepting external MODEM data or sequential encode tones are generated. Transmitter audio is fed, via the Control PWB, directly into the modulation circuits of the Analogue PWB without any filtering.

The Tx and Rx Audio enable lines operate at +5V logic levels whereas the switches require +8V logic levels. Level shift for each audio enable line, DEA and KEYLINE is provided by a section of IC2201. IC2201 is a Schmitt Trigger buffer. Hysteresis is provided via C2238, R2254, R2253, R2255.

DEA — Data Equipment Available - informs radio that external device is ready to accept data.

KEYLINE — An external PTT operated from within the External MODEM. Both KEYLINE and DEA are read on separate lines of the Control PWB Switch Input Register, and will only key the transmitter when a data call is in progress.

DCR — Data Channel Ready - signal to external device inviting data to be sent. DCR will not be in 'ready' state until the radio is transmitting. This line is buffered by TR2202.

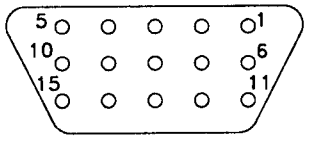
A +13V power source derived from the radio power supply is available for powering an external device. This supply is protected by a 250mA fuse.

Sequential Tone Encoding

Sequential signalling is controlled by the signalling microprocessor on the Control PWB. Encode tones are generated by the microprocessor on port 1 (pins 7, 8, 9), as a series of square-waves which are summed together by Digital-to-Analogue Converter (DAC) IC2202 and IC2203. The product is a 5-stepped squared waveform which is filtered by another stage of IC2203 to produce an acceptable sinusoidal waveform. The signal then passes via preset level potentiometer RV2201 (TONE DEVIATION LEVEL) before gating to the external Tx audio line.

Connections external to the radio are made by SKTG, which connects to a 15-way data socket (similar to the microphone connector). The pin numbering of the socket is as follows:

Pin Number	Connection
5	Rx Audio live
10	Rx Audio ground (analogue)
1	+13,6V
14	Tx Audio live
9	Tx Audio ground (analogue)
12	DCR (Data Channel Ready)
6	Keyline live
7	Keyline ground (digital)
11	DEA live
8	DEA ground (digital)



(VIEWED FROM FRONT)

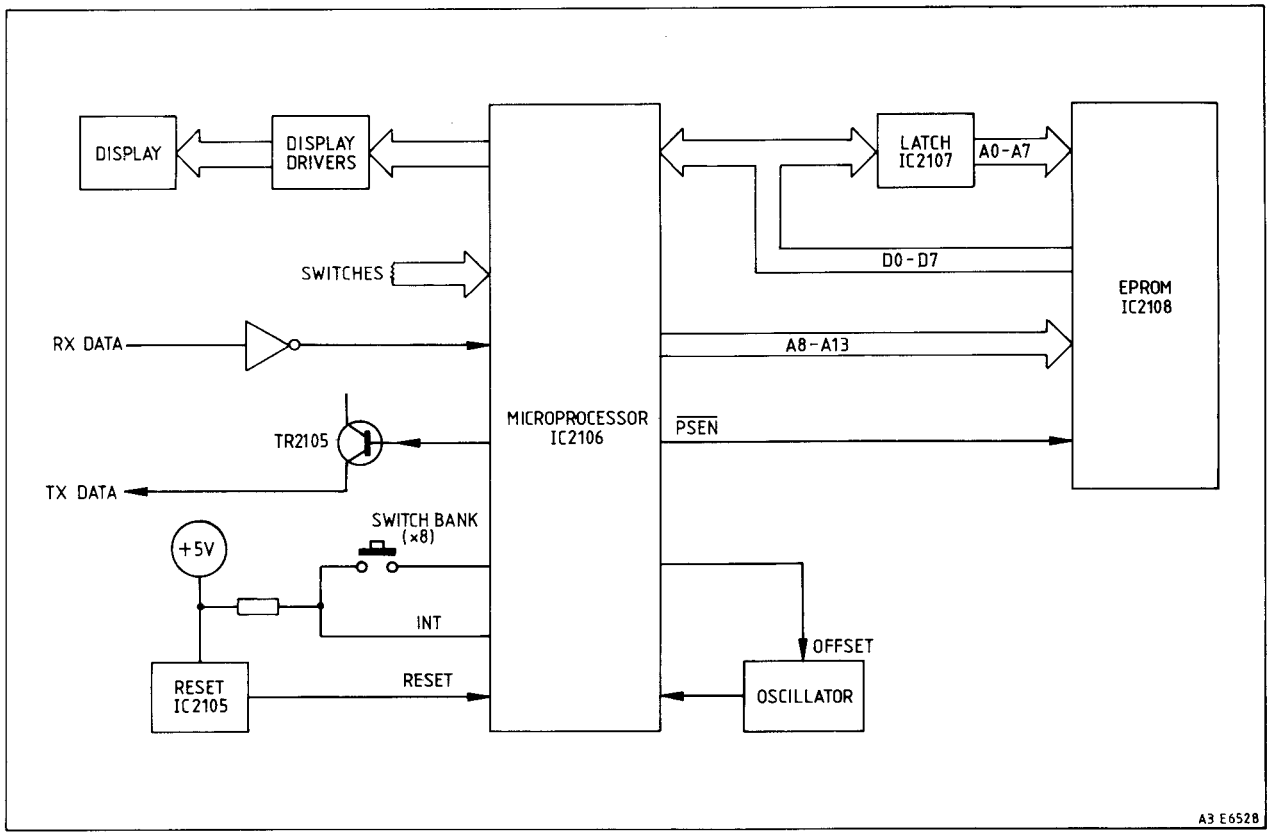


Fig 3.7 Standard Console Block Diagram

Microprocessor IC2106 receives and issues control information to and from peripheral devices. System operation is defined by a set of instructions either stored in EPROM IC2108 or masked within the processor, depending on the presence of R2103 or R2102. When R2103 is fitted, instructions are masked within the processor and IC2107 and IC2108 may be omitted from the PWB. When R2102 is fitted, instructions are read from EPROM IC2108.

Instructions within EPROM IC2108 are read by the microprocessor by first addressing the EPROM via the 8-bit latch IC2107 and then taking PSEN 'low'. Instructions are read and processed at a speed defined by the microprocessor crystal oscillator frequency and on-board oscillator-dividers. The microprocessor cycles through a loop until an 'interrupt' signal is received.

The microprocessor is reset at pin 10 by Reset chip IC2105 whenever the +5V regulated line drops below an acceptable level. The Console PWB has its own +5V regulator IC2104, which receives power from the transceiver 13,6V line at PLA1.

Two interrupt inputs to the microprocessor, INT0 and INT1, are held at +5V by R2105 and R2104 respectively. When a display button key is depressed, a 'low' is applied to the relevant input to inform the microprocessor to look for key switch action. Switches SW2102-SW2105 put an interrupt on IC2106 pin 14 (INT0) and switches SW2106-SW2109 put an interrupt on IC2106 pin 15 (INT1).

The microprocessor receives data from the transceiver which informs it as to whether clock offset is required for the current channel or not. If offset is required, the microprocessor puts a 'low' on TR2103 base via bridge R2116/R2115. This switches off TR2103 which in turn switches on TR2102, effectively putting C2117 in parallel with C2116 and pulling XL2117 down onto its calibration frequency. The frequency offset is not sufficient to disrupt the operation or timing of the microprocessor (see 'Control PWB').

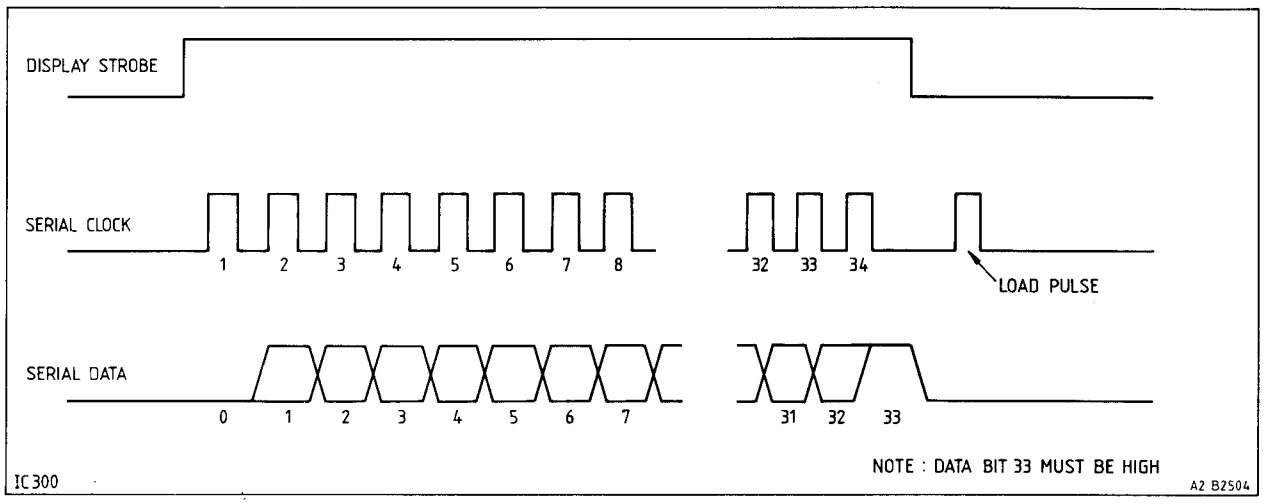


Fig 3.8 Display Driver Timing Diagram

For correct operation, LCD2101 requires a square-wave of approximately 50Hz which is applied to the LCD common backplane, with individual display segments driven in phase to switch them off, or out of phase to switch them on.

Two display drivers IC2101 and IC2102 are employed: these have a three line serial bus structure enabling serial data transfer from IC2106. Both have on-board oscillators; only that in IC2102 is used to drive the LCD backplane, the oscillator in IC2101 is disabled by grounding pin 3.

When the microprocessor makes the DISPLAY STROBE line high, data from the microprocessor is clocked into the driver by SERIAL CLOCK pulses, also provided by the microprocessor. Data is locked into the driver when the DISPLAY STROBE is low. At the 35th clock pulse the data is transferred to the LCD; LCD segments are switched on as a result of corresponding 'high' serial data bits. As data is locked into the driver, the display is updated only when display information needs to be changed, ie as a result of pressing a console button.

The display backlight is switched on and off by the microprocessor via IC2103a,b,c, and TR2104.

SECTION 3
TECHNICAL DESCRIPTION

CIRCUIT SUMMARY

Introduction

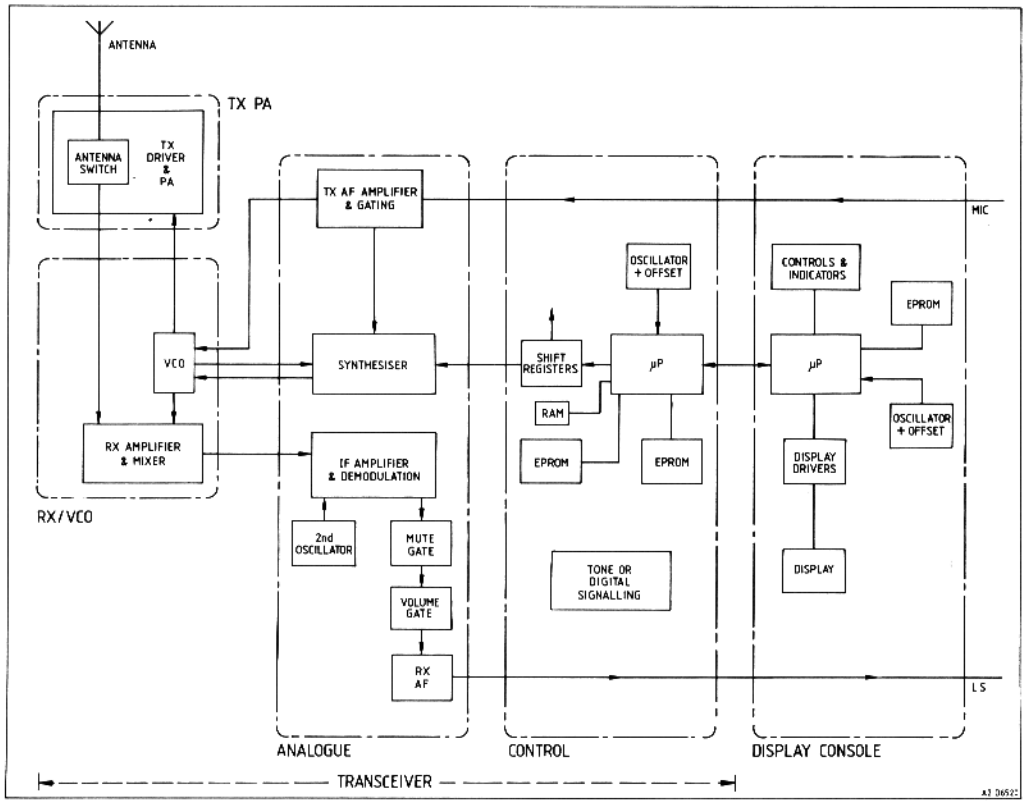


Fig 3.1 Basic Transceiver Block Diagram

The transceiver consists principally of five PWB assemblies as follows:-

Tx PA — comprising antenna switch, Tx driver & PA.

Rx/Tx RF — comprising RF Amplifier (UHF bands only), electronically-tuned RF filter, 1st Mixer, Rx/Tx VCO (VHF) or separate Rx and Tx VCOs (UHF), and RF tracking circuits.

ANALOGUE — comprising:-

- Synthesiser:- Reference Oscillator, Comparator and Dividers, Pre-Scaler, synthesiser IC, Loop Filter.
- Transmitter:- Audio amplifier, limiter, filters and gating. Power Control circuits.

	Receiver:-	1st & 2nd IFs, 2nd oscillator & mixer, Rx demodulation circuits including squelch gate. Digital AF volume control. AF Amplifier, filters and gating.
CONTROL	comprising main transceiver microprocessor with clock oscillator, EPROM, EEPROM, RAM, Shift Registers, timers, 30V generator and tone signalling circuits.	
DISPLAY CONSOLE	comprising (slave) microprocessor, EPROM, address latch, front panel controls and indicators, liquid crystal display and associated display drivers.	

Microprocessors

Virtually all transceiver functions are controlled by a microprocessor which receives and issues control signals to and from peripheral devices. System operation is defined by a set of instructions stored in an EPROM. In order to maintain a compact transceiver layout avoiding additional and cumbersome wiring, the interface between processor and peripheral devices is of the serial data type; shift registers are employed to convert serial data to parallel data when required.

The processor derives a clock signal from an external oscillator. The output frequency of the oscillator can be offset by software should a harmonic from it fall within any of the programmed receiver channels. This offset is not significantly great to affect the operation of the microprocessor.

The microprocessor selects programmed channels, switches the VCO range and causes the channel number to be displayed. The same data is used to provide an automatic increment or decrement to the nearest programmed channel whenever the channel change function is operated.

Channel changing is prompted by user action on the transceiver console. The microprocessor addresses and monitors channel information stored in EEPROM. This information is sent via shift registers to the synthesiser where it sets the division ratio of the dividers.

A second (slave) microprocessor is employed within the transceiver for generation of tone-signalling, receiving instructions from, and sending status information to, the master processor. A third microprocessor is used in the 4-Digit console as an interface between the master processor and console front panel.

A connection to the transceiver's external message bus can be made via the front panel socket to allow alterations to customizable data stored within the EEPROM. Such alterations must be valid configurations and are subject to programmer authority.

Synthesiser

The synthesiser is of Phase-Lock Loop (PLL) type, employing a reference oscillator, voltage controlled oscillator (VCO) and comparator. The VCO feeds a sample of its output via a prescaler and dividers to a comparator. Here the sample output is compared against a reference source, and outputs an error voltage to re-adjust the VCO if it is out-of-lock.

A loop filter attenuates high frequency noise and is the main element that determines the dynamic characteristics of the phase locked loop (PLL). AF modulation is applied to both the VCO and the reference oscillator to reduce audio frequency components at the phase comparator output and to provide a low modulation frequency response.

The synthesiser output is used to provide the receiver local oscillator frequency in the receive mode and the modulated carrier source for the transmitter. Both signals are passed through buffer stages and are normally at final frequency.

Transmitter

Audio signals from the transceiver microphone input are amplified and fed via a pre-emphasis circuit to the limiter. The limiter ensures that system deviation is not exceeded despite wide variations in microphone output level. From the limiter the signal is fed via a low-pass filter with a 3kHz cut-off to the Reference Oscillator and VCO Loop Filter. A separate audio input is provided on the Transmitter audio amplifier for in-band tone-signalling. This input by-passes the part of the microphone amplifier stage switched off for the duration of the tone encode period, thereby ensuring that speech does not interfere with the tone information.This does not apply to DTMF tones which are generated from within a keypad microphone.

Output from the VCO, at final carrier frequency, is applied via a buffer-amplifier before application to the PA. The transmitter PA circuit is of broad-band design, its gain controlled by a feedback power control circuit. Any one of six power levels may be specified on a per-channel basis. Transmitter power is adjustable between 1W and either 25W or 30W, dependant on frequency band.

Power Amplifier RF output is fed to the antenna switch, where the signal is directed by diode switches to the antenna filter and antenna socket. The antenna filter comprises a low-pass filter to reduce harmonic radiation.

The transceiver may be programmed to disable the transmitter at a pre-determined period after key-on. The timer is reset by releasing the PTT switch.

Receiver

Signals from the antenna socket are directed by diode switches in the antenna switch to the input of the electronically-tuned filter which provides a high degree of selectivity against unwanted signals. Use of varicap diodes allow the pass-band of the filter to be tuned to any part of the frequency band. UHF band versions have an amplifier to boost the filtered output. The amplified and/or filtered RF signals and VCO output from the synthesiser are combined in a mixer stage to produce a 21,4MHz intermediate frequency.

In the receive mode, the synthesiser circuits are programmed to produce an output from the receiver VCO at the following frequency:-

EO Band: $f_o = f_c + 21,4MHz$

All other Bands: $f_o = f_c - 21,4MHz$

where f_o = oscillator injection frequency and
f_c = channel centre frequency.

The mixer output is fed via suitable matching to the 1st IF Crystal Filter on the Analogue PWB, which provides selectivity against adjacent channel interference. The filtered 21,4MHz signal is amplified and fed to a 2nd mixer stage, together with a crystalled controlled second oscillator to produce a 2nd IF signal of 455kHz. Crystal frequencies for the 2nd oscillator are 20,945MHz (standard) and 21,855MHz (alternative). The 455kHz signal is amplified and then demodulated to provide a low-level audio output. This is fed via a digital attenuator controlled by the processor which provides stepped volume level control, before application to the receiver audio amplifier. A squelch circuit, driven by the noise output of the demodulator, is used to inhibit receiver noise reaching the loudspeaker when a carrier signal is absent. Squelch threshold level is controlled by software.

An RSSI (received signal strength indicator) can be used for receiver voting or trunked radio applications, in addition to driving the signal strength indicator on the console display.

CONTROL PWB

Microprocessor

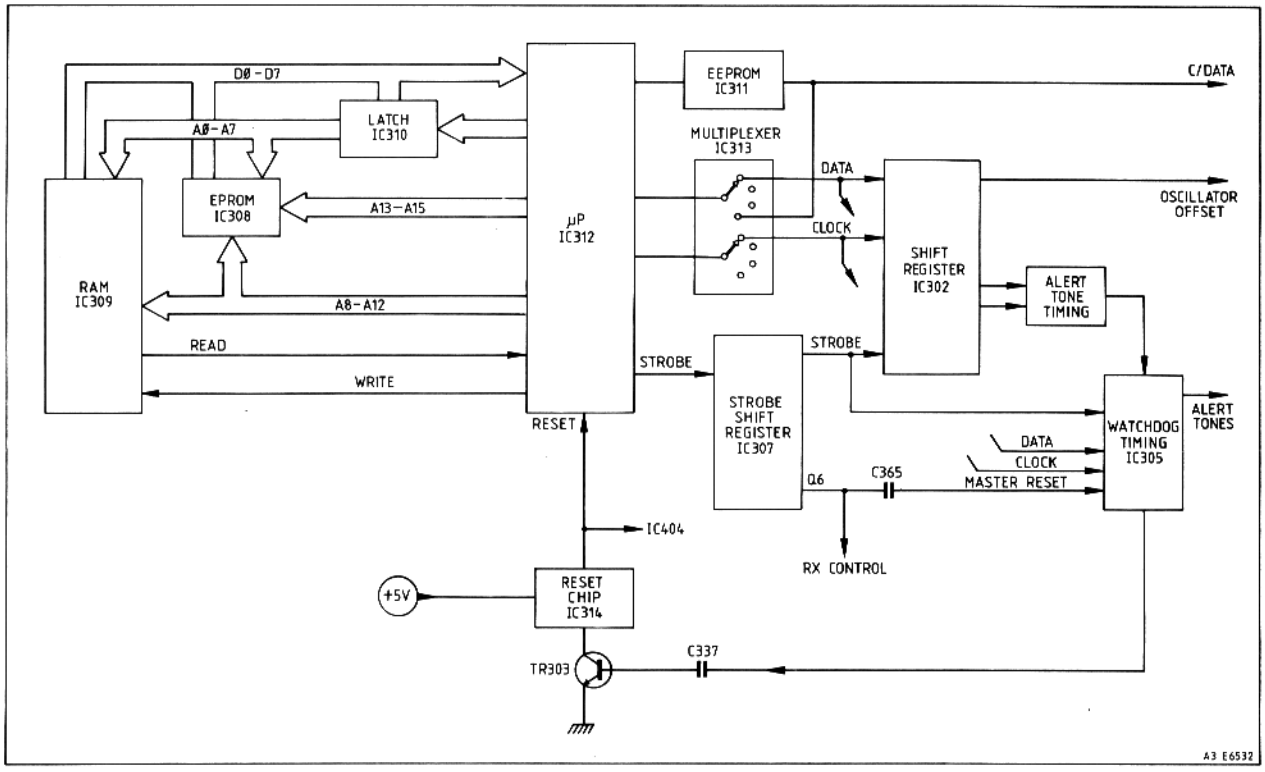


Fig 3.2 Microprocessor Block Diagram

The power-up process, which includes the microprocessor "self-check" routine, takes about four seconds. Operation of the transceiver controls will be ignored by the microprocessor during this period.

Microprocessor IC312 receives and issues control information to and from peripheral devices. System operation is defined by a set of instructions stored in EPROM IC308 or RAM IC309. These instructions are read by the microprocessor by first addressing either the EPROM or RAM via the 8-bit latch IC310 and then taking PSEN 'low'. Instructions are read and processed at a speed defined by the microprocessor crystal oscillator frequency and on-board oscillator-dividers. The microprocessor cycles through a loop interrogating peripheral devices until a message is received.

EEPROM IC311 is a serial device and is thus slow to exchange and update data. Therefore at switch-on, microprocessor IC312 loads EEPROM (IC311) data into RAM IC309, which, although having a volatile memory, is a parallel device capable of faster data transfer. At switch-off, the microprocessor interrogates the RAM for any changes made to stored data (channel number selection, volume control setting etc) and writes any modifications to the EEPROM. If significant changes have been made, there is a noticeable delay before the microprocessor issues instructions to remove power from the transceiver.

Data stored within the 512 byte EEPROM is typically as follows:

Transmit and receive frequencies for channels 0 - 9

Encode and Decode Identities 1 - 4

Last channel number used

Last volume control setting

Frequencies for channels 10 - 99 and Encode/Decode identities 5 - 8 are stored in EPROM IC308. The microprocessor reads EPROM/RAM channel frequency data and whether clock offset is required for the current channel or not. If offset is required, the microprocessor instructs shift register IC302 to put a 'low' on Q1 (pin 4) which is then applied to TR307 base via bridge R356/R357. This switches off TR307 which in turn switches on TR306, effectively putting C334 in parallel with C333 and pulling XL301 down in frequency onto its calibrated frequency (12MHz). Offset is implemented on a channel by channel basis, whenever the receiver channel is within ±50kHz of a 0,5MHz multiple. The frequency offset is sufficient to move any oscillator harmonics away from a programmed receiver channel, but insufficient to disrupt the operation or timing of the microprocessor.

Multiplexer IC313 allows IC312 to read and write data to and from various peripheral devices in a number of modes. They are:-

(i) Internal Message Bus - Serial TxData and RxData to SELCALL microprocessor IC404

(ii) Internal Expansion Bus - Clock and Data lines to Shift Registers on Analogue PWB.

(iii) External Message Bus - TxData and RxData to external devices, eg console, PDP, CDP, microcomputer etc. *(Intel 8051 Mode 2)*

(iv) External Expansion Bus - Read/write to shift registers external to Analogue PWB, DTMF/keypad microphone. *(Intel 8051 Mode 0)*

The microprocessor writes, via multiplexer IC313, to Shift Registers IC302, IC307 and IC503. Data is distributed as follows:-

Shift Register IC302

Q1 Microprocessor crystal oscillator frequency offset*
Q4 Relay Start*
Q5 Alert Tone frequency*
Q6 CTCSS Detector output gate (see "CTCSS Signalling")
Q7 Alert Tone Output gate*
Q8 Alert Tone frequency*

* See "Power-Up and Alert Tone Generation"

Shift Register IC307

Q1 Strobe for Shift Register IC302
Q2 Strobe for Shift Register IC503
Q4 Load Switch Input Register IC303
Q5 Synthesiser Control (Analogue PWB)
Q6 Rx Control Data (Volume Control and audio gates)ǂ
Q7 Tx Power Level Controlǂ
Q8 Tx Control (VCO Tx/Rx and audio gates)*

ǂ Analogue PWB

Data is read into the microprocessor from the following input registers:-

A to D Converter IC301

A0 Tune Volts
A1 +13,6V voltage sense.
A2 Tx Temperature (via Analogue PWB, from TH1 mounted on heatsink)
Q3 Noise Level (squelch output from IC207, Analogue PWB)
Q4 RSSI (from IC201 pin 11, Analogue PWB)
Q5 Power Level (from Power Control circuit, Analogue PWB)
Q6 Volume
Q7 Hook/Facility Switch

Switch Input Register IC303

D0 ON/OFF Switch.
D2 PTT Switch.
D3 Remote Alarm (External connection to radio)
D5 Synthesiser in/out lock.
D7 CTCSS Valid (see "CTCSS Signalling")

Power-Up and Alert Tone Generation

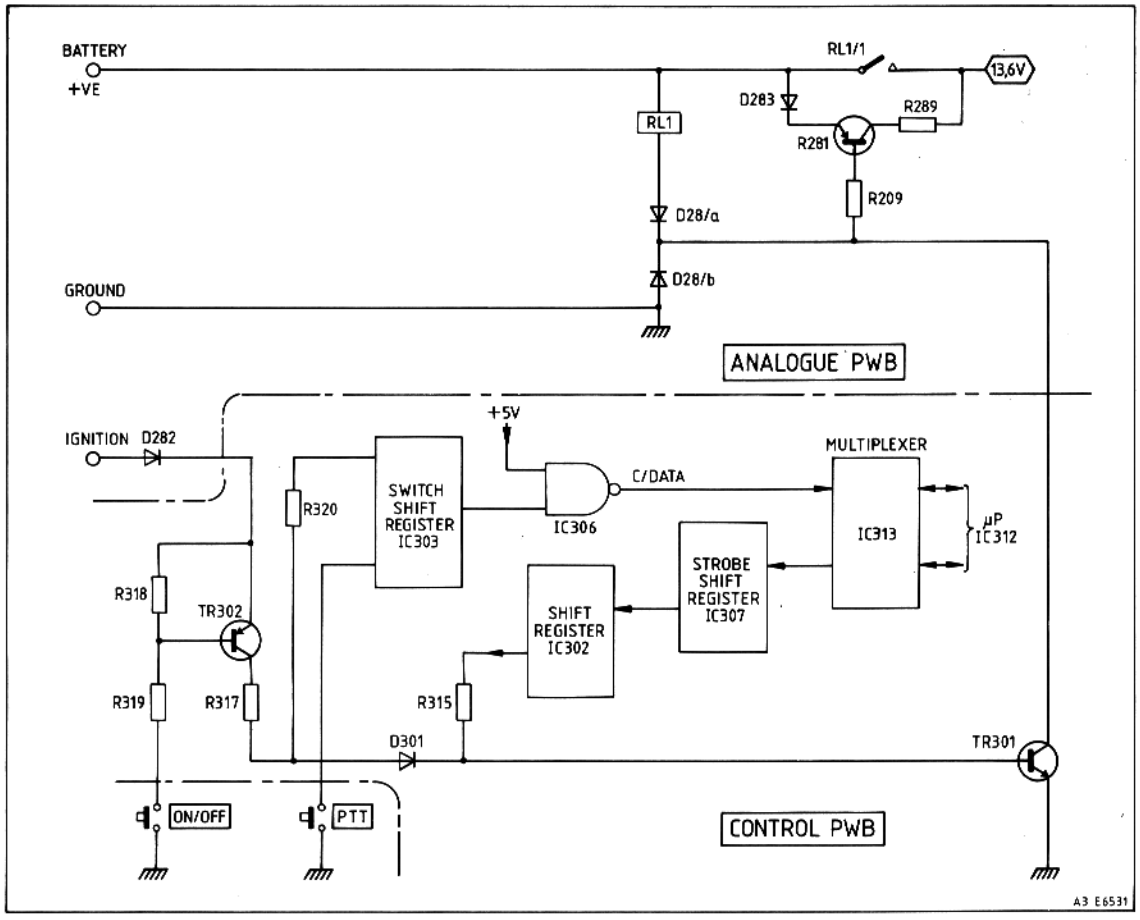


Fig 3.3 Power-Up Block Diagram

Reset chip IC314 generates a reset pulse for the microprocessor which is output at pin 6. A reset is generated at power-up, whenever the +5V line drops below a threshold level, and whenever the Watchdog/Timer IC305 outputs a reset signal.

The Watchdog/Timer IC monitors activity on the receiver control line (IC307 pin 13) and if a pre-defined period of inactivity is observed, assumes that IC312 has locked-up and outputs a reset signal via TR303 to IC314 pin 2. Alert Tone generation is performed by IC305. Tone frequencies are determined by resistors switched in and out of the IC305 feedback circuit by isolation gates IC304a,b, and tone duration determined by gate IC304c. The gates are switched by Shift Register IC302, acting on data sent by microprocessor IC312.

When the ignition input line to the transceiver is pulled up to +12V, the voltage is applied to TR302 emitter. When the ON/OFF switch is set by the user to ON (switch closed), a 'low' is applied to TR302 base. This action switches on both TR302 and TR301 (via D301) to energise the Start Relay situated on the Analogue PWB. The 'high' on TR302 collector is also applied to Switch Input Register IC303, at pin 11, which is transferred as data, via IC306c, to microprocessor IC312. Once the microprocessor has acknowledged user action to switch on the unit, it instructs Shift Register IC302 to output a 'high' at pin 7 (Q4) to maintain the 'on' condition of TR302. Once this is done, the radio may only be switched off when the microprocessor sets Q4 to 'low', normally after the input to IC303 has gone 'low'. The microprocessor waits for the EEPROM to be updated by changes in RAM data before sending switch-off data.

30V Generation

The Tuning Law circuits and Loop Filter require +30V DC to provide sufficient voltage swing for complete frequency band coverage. This is generated on the Control PWB by oscillator IC318. Output at pin 6 is rectified by D310 and smoothed by C348, R373 and C349. A sample of the output, produced by R371, RV301 and R372, is applied to pin 1 of IC318 as feedback to provide a degree of adjustment of the output level.

Synthesiser

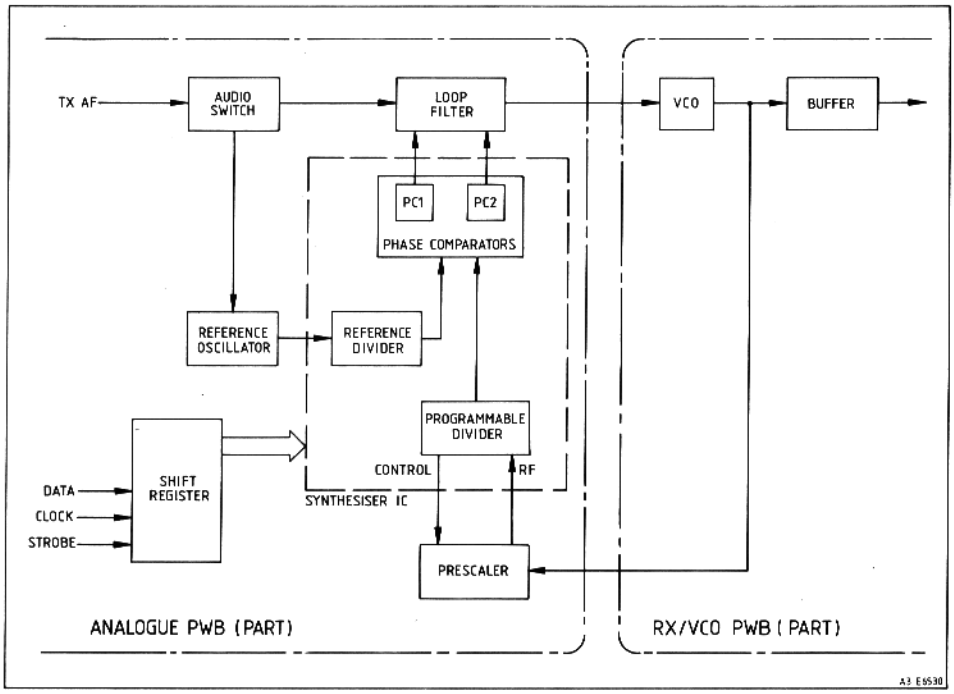


Fig 3.5 Synthesiser Block Diagram

The synthesiser is of a single-loop type with a VCO operating at either the transmitter channel frequency or receiver local oscillator frequency depending on whether the transciever is transmtting or receiving. All the transmitter and receiver frequencies are controlled by a single high stability crystal-controlled reference oscillator. On transmit, audio is applied to both the VCO (via the loop filter) and the reference oscillator, to prevent cancellation of the modulation by the phase comparator.

The reference oscillator TR132, is a Colpitts oscillator, with crystal XL131 running in series resonance mode. TR131 completes the feedback loop. Normally a crystal frequency of 8,4MHz is used, but where the receiver frequency (on any channel) is within ±50kHz of a multiple of the reference crystal frequency, alternative frequencies of 7,2MHz, 7,8MHz or 9,0MHz are used. To minimise long term drift, the crystal is pre-aged. A multi-turn potentiometer, RV131, is used to trim the reference frequency, and hence the transmit and receive frequencies, to the required values. Oscillator output is applied to IC104 pin 8.

Status of the Q outputs from Shift Register IC105 control the division ratio of IC104 reference divider. The reference frequency input to the phase comparators (the output from the reference divider) is either 5kHz (for 20kHz or 30kHz channel spacing) or 6,25kHz (for 12,5kHz or 25kHz channel spacing).

The phase comparators require two input signals, one from the reference divider and the other from the VCO programmmable divider. The programmmable divider, together with Prescaler IC102 enables the VCO output frequency to be changed in steps equal to the equipment channel spacing. There are two phase comparators, PC1 and PC2, and both compare the phase of the two divider outputs.

Phase comparator PC1 is a high gain sample-and-hold comparator which gives good noise performance but is slow to acquire lock. Phase comparator PC2 is a low gain digital comparator which is able to acquire lock rapidly but is noisy. IC101 circuitry is arranged so that phase comparator PC2 rapidly brings the loop into the linear range of PC1 and then goes tri-state. In this way, the loop is able to acquire lock rapidly whilst maintaining the good noise performance of PC1.

The loop filter is a conventional low-pass filter using operational amplifier IC103b. The filtered output is available as the control voltage for the VCO (VHF) or VCOs (UHF) at PLF3 (TUNE VOLTS). In order to produce the necessary control voltage range, IC103 operates from the 30V supply generated on the Control PWB. A buffer, IC103a, provides a TUNE VOLTS output suitable for the Control PWB microprocessor, at PLA12.

An out-of-lock signal ('low') is presented at IC104 pin 3 until phase comparator PC2 goes tri-state. This is applied to the switch input shift register ICxxx, as control data for microprocessor ICxxx, and to TRxxx, LEDxxx as a visual indication of lock for fault finding purposes.

Two types of prescaler are used, depending on frequency band; VHF band equipments use a prescaler with an 80/81 division ratio, while UHF band equipments use a prescaler with a 128/129 division ratio. The prescaler is of the two modulus type and its division ratio is controlled at pin 8 by synthesiser IC102. A sample of VCO output is applied via PLE1 to the prescaler at pin 5 (pin 2 on UHF prescalers). The prescaler output is divided down (within IC102) to the same frequency as the reference oscillator frequency; the required division ratio equalling the prescaler output frequency divided by the phase comparator reference frequency (6,25kHz or 5kHz).

Transmitter Switching

Transmit/receive switching data from the Control PWB is sent to Shift Register IC2 and is output at pin 11 (Q8) as a 'high' level for transmit and 'low' for receive. A 'high' will switch on TR3 and hence TR2 (via D2) and TR1. Transistor TR2 switches +10V DC to the Tx pre-amplifier stages via PLC1 and TR1 switches current to the antenna pin-diode switches via PLC7. Double-diode D1a,b controls the voltage drop on TR1 base and hence limits the current to the pin-diodes.

At switch-on, TR4, TR3 hold the radio in the receive mode momentarily, in order to allow all device gates to set to their correct 'state'. This 'hold' time is determined by the time constant of R27, C17.

Transmitter Power Control

Power Level Data from the Control PWB is output from Shift Register IC2 between gates Q1 to Q7 and is applied to the D to A converter comprising resistor array RN1 and operational amplifier IC1d. Output from IC1d is fed to buffer TR8, calibration potentiometer RV1 and operational amplifier IC1c, before application as a reference level for comparator IC1a at pin 3. Temperature compensation is added by IC1c, R22, D6, as the Schottky diodes in the power detector circuits do not have a linear response.

To prevent spurious power-settings, R16, C10 provide smoothing for the reference level.

Output from the Tx PA Schottky diode detectors (Tx Detector Output) at PLC3 is buffered by IC1b before application to the second comparator input at IC1a pin 2. IC1a output is applied to TR5-7 and to the Control PWB input register via PLB6. Transistors TR7, TR6, TR5 form a DC amplifier which produces a DC output suitable to drive the TX PA driver devices. Potentiometer RV2 limits the maximum control output voltage available. Diode D5 provides temperature compensation for TR7, and D7 holds TR7 emitter voltage "up" when the amplifier stages are in limiting.

Bias for the Schottky diodes is provided by R24, R25, and is presented to the Tx PA via PLC2.

Logic levels required from IC2 output gates for specified transmitter power levels are given at the end of Section 4.

Transmitter Audio

Signals from the microphone are applied via the Control PWB to PLA4 and fed to operational amplifier IC55a. Amplifier gain is adjusted by RV53 to compensate for variations in microphone sensitivity. Further amplification is provided by IC55b. The audio signal is then applied to IC55c which adds a 6dB/octave pre-emphasis characteristic and limiting to the signal. The output is applied to a 2nd order Chebishev (Tchebishev) filter, which has a very sharp cut-off profile. Audio is then output to IC53a,b, a 4th order Butterworth filter, which in combination with IC55c, produces a flat in-band response with a good high frequency roll-off characteristic.

Signalling tones are applied to the AF stages via IC52a, which is controlled by pin 13 (Q6) of Shift Register IC54. As these signals are on a low impedance line, their connection to resistive bridge R67, R64, attenuates speech output and thus prevents over-modulation during tone transmission.

When in-band tones (eg SELCALL) are being transmitted, IC54 pin 12 (Q7) goes 'low', disabling transmission gate IC52b, inhibiting microphone audio from the remainder of the audio stages and thus preventing speech corrupting out-going tone information. When speech is allowed to pass the transmission gate, IC55d output is attenuated by R70, R69, before application to IC53a.

The combined audio sources are then filtered by IC53a, b & c. Where group delay is a critical factor (eg digital signalling in FM1200 variants) signals are applied to IC53c via transmission gate IC52d. Modulation level is adjusted by RV52.

Audio is then passed to IC51a, a buffer amplifier whose output is applied to the VCO modulator and IC51b which provides a buffered output for the reference oscillator. Potentiometer RV51 provides modulation balance, by adjusting the audio level to the reference oscillator.

Receiver IF and AF

FL301 is a six-pole crystal filter which provides a high degree of selectivity against unwanted adjacent channel signals. Output from FL301 is then fed via pre-amplifier TR201 to the input of IF Amplifier/Demodulator IC201. Diodes D201a,b limit the signal to prevent overloading IC201 input.

IC201 provides further amplification of the 21,4MHz signal before application to the internal 2nd mixer, where the signal is converted to 455kHz. The second mixer oscillator is external, comprising TR202, XL201 running at 21,855MHz (standard) or 20,945MHz (alternative) and is applied to IC201 at pin 19. The product is then fed through external 455kHz ceramic filter FL202 and then returned to IC201 which provides 2nd IF amplification and demodulation. A quadrature detector is employed in IC201, and is tuned by external quadrature coil L202. There is also a RSSI output on IC201 at pin 11.

Demodulated audio output from IC201 pin 4 is then applied to IC202b, a low-pass filter with a 120kHz cut-off which removes any 455kHz signal component and harmonics. The audio signal then is fed through limiter IC202c which removes high impulse noise before application to isolation gate IC204b, which, when a 'high' is applied to pin 5, breaks the signal path to pin 2 of IC203a should tone-signalling control of the receiver be required. Audio for the tone-signalling circuits (incorporated on the Control PWB) is taken from the junction of R225, R223. Audio is returned from the tone-signalling circuits (subject to signalling control status) via R268, C224. Buffer IC203a sets the HF response of the audio signal by introducing a 6dB/octave de-emphasis characteristic. Audio is then applied to the external isolation gates IC204d and IC204e, which, if required, breaks the direct signal path to IC203d, allowing audio to be re-directed, or processed, by an external stage via the external options connector PLJ.

A high-pass filter, IC203d, shapes the LF audio characteristic by providing a 300Hz roll-off, and after passing through the receiver mute gate IC204a, is applied to the low-pass filter IC203c, which provides a 3kHz cut-off.

Control of the audio gain level is provided by a four-stage electronic volume control comprising transistors TR203-TR206 which switch resistive attenuators in or out, according to voltages to their bases by shift register IC205. A preset (master) volume control is provided by RV203, TR207.

Final amplification is carried out by power amplifier IC206; its output is presented at PLB10 where it is directed via the Control PWB to connectors at the front and rear of the transceiver.

A portion of the output from IC202b pin 7 is applied to noise squelch circuits IC202a, IC202d, IC207. IC202a is a high-pass filter with a 35kHz cut-off and IC202d a high-gain amplifier which is controlled by thermister TH201. The filtered and amplified noise output is then directed through the active rectifier stage IC207a, D203a, D203b to the active smoothing stage IC207b,c,d. Overall gain is adjusted by preset RV204 and the output is applied to PLB1.

TRANSMITTER POWER AMPLIFIERS

All frequency band versions of the PWB are of untuned broadband circuit design. All buffer stage input and output impedances are close to 50Ω to improve broadband performance. Connections between pre-amplifier, driver and power amplifier devices are made via multiple-section matching networks and printed circuit microstrips.

Transmitter PA AT29027 (E0 Band)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of 0dBm to buffer amplifiers TR705, TR704, which receive their DC supply from the Tx Switched +10V line. The signal is then amplified by pre-amplifier TR703, driver TR702 and power amplifier TR701. TR703 and TR702 receive their DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to their collectors. PA transistor TR701 is powered from the +13,6V line.

The signal, at final carrier power, is applied via low-pass filter C706, L703, C705, C704, L702, C703, C702, L701 and C701, to the antenna socket.

Schottky diodes D703a,b are connected to each end of L707, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L707, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D701 and D702, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Transmitter PA AT29025/- (A9, B0, Bands)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of 0dBm to buffer amplifiers TR904, TR903 and preamplifier TR902, which receive their DC supply from the Tx Switched +10V line. The signal is then amplified by driver TR901 and power amplifier TR900. TR901 receives its DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to its collector. PA transistor TR900 is powered from the +13,6V line.

The signal, at final carrier power, is applied via low-pass filter C906, L902, C905, L901, C903, L900 and C901, to the antenna socket.

Schottky diodes D902a,b are connected to each end of L906, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L901, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D900 and D901, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Transmitter PA AT29026/- (K1, K2 Bands)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of 0dBm to buffer amplifiers TR1004 and TR1003 which receive their DC supply from the Tx Switched +10V line. The signal is then passed to pre-amplifier TR1002, driver TR1001 and power amplifier TR1000. TR1002 and TR1001 receive their DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to their collectors. PA transistor TR1000 is powered from the +13,6V line.

The signal, at final carrier power, is applied via low-pass filter C1006, C1005, L1002, C1004, L1001, C1003, C1002, L1000 and C1000, to the antenna socket.

Schottky diodes D1002a,b are connected to each end of L1005, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L1001, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D1000 and D1001, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Transmitter PA AT29028/- (UHF Bands)

Drive from the Rx/VCO PWB is applied via PLD3 at a level of +8dBm to buffer amplifiers TR1205 and TR1204 which receive their DC supply from the Tx Switched +10V line. The signal is then passed to pre-amplifier TR1203, driver TR1202 and power amplifier TR1201. TR1203 receives its DC supply from the Tx Power Level Control line, and hence transmitter power is ultimately determined by the voltage level applied to its collector. Driver TR1202 and power amplifier TR1201 are powered from the +13,6V line.

On 6 watt versions of the PWB, power amplifier TR2101 is omitted and link LK1201 added to carry the signal to the antenna filter. The matching networks for TR2101 are also omitted to maintain 50Ω impedance at TR2102 output.

The signal, at final carrier power, is applied via low-pass filter C1207, C1206, L1203, C1205, L1202, C1204, C1203, L1201, C1202 and C1201, to the antenna socket.

Schottky diodes D1203a,b are connected to each end of L1206, which produces a nominal 90° phase shift across its terminals at mid-band frequencies. Thus, even in VSWR mis-match conditions, if a null is detected at one end of L1206, a peak should be detected at the other end. Outputs from the diodes are summed and hence the detector output level is determined by the diode providing the higher DC level. Bias for the Schottky diodes is supplied at PLB5 (from the Analogue PWB).

On receive, signals from the antenna are fed through the three-stage antenna low-pass filter to the pin-diode antenna switch. The Antenna Switch Control line (PLB1) will be 'low' on receive, switching off D1201 and D1202, and hence directing received signals to the RF input on the Rx VCO Assembly via PLA1.

Provision for resistive attenuation is made on the Tx PA PWB for when de-sensitizing of the receiver is required; however in most applications this feature is not required and the resistors are omitted.

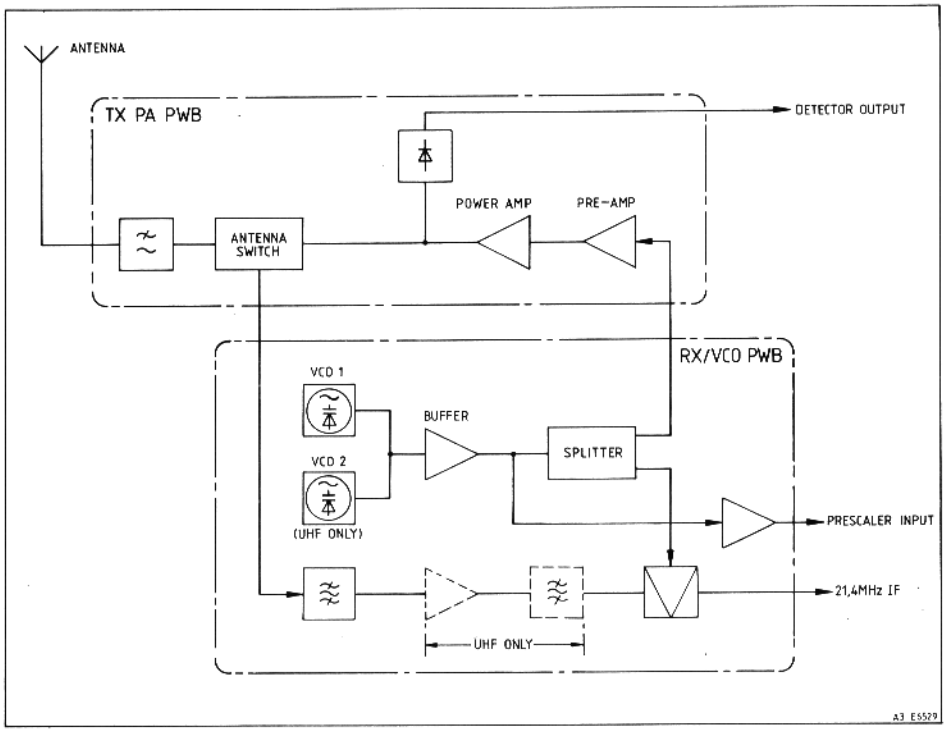


Fig 3.6 Transceiver Front End Block Diagram

Rx VCO ASSEMBLY AT29029/- (E0 Band)

Signals for the receiver from the PA antenna switch are applied to L602. Provision for resistive attenuation is made on the Rx VCO Assembly where de-sensitizing of the receiver is required; however in most applications this feature is not required and the resistors are omitted. The required selectivity is provided by a 4-pole electronically-tuneable filter comprising varicap diodes D600 - D618 and associated components; the varicap diodes are arranged in a back-to-back format to minimise distortion of the tuned signal. As the varicap diodes must be finely-matched to provide accurate tracking over the entire frequency band, four unused and similarly-matched varicap diodes are provided on the PWB assembly for spares, obviating replacement of all varicap diodes in the event of the failure of one.

The filtered signals are then applied to g1 of dual-gate MOSFET TR601. Local oscillator output, at 21,4MHz above receiver carrier frequency, is applied to g2 of TR601 and the product is output at its drain. Resistor R609, inductor LV601 and capacitors C601, C604 provide suitable matching for the 21,4MHz crystal filter on the Analogue PWB.

Oscillator output is taken from TR653 source and is fed via C662 to buffer TR654, a dual-gate MOSFET, whose output, provides oscillator output via C668 to amplifier TR657. A Wilkinson Splitter, formed by C673, L657, C674, and L658, C675, splits power from TR657 collector equally to each end of R674. Signal level at the injection coil L605 is typically +8dBm, which is suitable for application to the 1st mixer TR601. However, the transmitter power amplifier requires a level of 0dBm, and thus the signal from L658 is attenuated by R675, R676, R677.

A sample signal from TR854 drain is provided for the Prescaler via C664, TR656, and is presented at PLA4.

The Voltage Translation circuit comprises IC601 and is powered by the 30V line from PLA13. The latter part of IC601 controls the set-point and slope for the tuning law; RV601 alters the slope. Typical tuning voltage range is 8-20V. When the transceiver is transmitting, TR602 is switched on by the VCO Tx/Rx control line, pulling the translation output down to 0V, and hence de-tuning the receiver band-pass filter.

Rx VCO ASSEMBLY AT29029/- (A, B, K Bands)

Signals for the receiver from the PA antenna switch are applied to L802. Provision for resistive attenuation is made on the Rx VCO Assembly where de-sensitizing of the receiver is required; however in most applications this feature is not required and the resistors are omitted. The required selectivity is provided by a 4-pole electronically-tuneable filter comprising varicap diodes D800 - D815 and associated components; the varicap diodes are arranged in a back-to-back format to minimise distortion of the tuned signal. As the varicap diodes must be finely-matched to provide accurate tracking over the entire frequency band, four unused and similarly-matched varicap diodes are provided on the PWB assembly for spares, obviating replacement of all sixteen diodes in the event of the failure of one.

The filtered signals are then applied to g1 of dual-gate MOSFET TR800. Local oscillator output, at 21,4MHz below receiver carrier frequency, is applied to g2 of TR800 and the product is output at its drain. Inductors LV801, L806 and capacitors C811, C814 provide suitable matching for the 21,4MHz crystal filter on the Analogue PWB.

VCO frequency coverage is determined manually by CV858 and electronically by varicap diodes D851, D852. Modulation compensation is provided by D853. To maintain frequency stability, a ripple-free power supply must be provided for the VCO, and the supply line from the Analogue PWB is smoothed further by capacitance multiplier network C860, R857, TR853.

The VCO Tx/Rx line (PLA6) is 'low' for receive, thus switching on TR850, switching off TR851 and D850. This effectively adds the inductance of L851 in series with L852, pulling JFET oscillator TR852 down in frequency, so that the local oscillator can track 21,4MHz below the receiver carrier frequency. When the transceiver is keyed to transmit, the VCO Tx/Rx line is 'high', switching on D850 which decouples L851 via C851, so that L852 is the only resonant inductance.

Oscillator output is taken from TR852 source and is fed via C862 to buffer TR854, a dual-gate MOSFET, whose output, provides oscillator output via C868 to amplifier TR856. A Wilkinson Splitter, formed by C874, L857, C875, and L858, C876, splits power from TR856 collector equally to each end of R874. Signal level at the injection coil L801 is typically +8dBm, which is suitable for application to the 1st mixer TR800. However, the transmitter power amplifier requires a level of 0dBm, and thus the signal from L858 is attenuated by R875, R877, R876.

A sample signal from TR854 drain is provided for the Prescaler via C865, TR855, and is presented at PLA4.

The Voltage Translation circuit comprises IC800 and is powered by the 30V line from PLA13. The latter part of IC800 controls the set-point and slope for the tuning law; RV801 alters the slope, RV802 sets the level. Typical tuning voltage range is 8-20V. When the transceiver is transmitting, TR801 is switched on by the VCO Tx/Rx control line, pulling the translation output down to 0V, and hence de-tuning the receiver band-pass filter.

Rx VCO ASSEMBLY AT29031/- (UHF Bands)

Signals for the receiver from the PA antenna switch are applied to L1101. The required selectivity is provided by a 2-pole electronically- tuneable filter comprising varicap diodes D1102 - D1109 and associated components; the varicap diodes are arranged in a back-to-back format to minimise distortion of the tuned signal. The signals are then amplified by TR1101, a gallium-arsenide dual-gate MESFET, before application to a 4-pole tuneable filter comprising D1110 - D1125. Again the diodes are arranged in a back-to-back format. As the varicap diodes must be finely-matched to provide accurate tracking over the entire frequency band, four unused and similarly-matched varicap diodes are provided on the PWB assembly for spares, obviating replacement of all varicap diodes in the event of the failure of one.

The filtered signals are then applied to g1 of dual-gate MOSFET TR1102. Local oscillator output, at 21,4MHz below receiver carrier frequency, is applied to g2 of TR1102 and the product is output at its drain. Inductor LV1101, and capacitors C1146, C1147 provide suitable matching for the 21,4MHz crystal filter on the Analogue PWB.

Frequency coverage of the JFET receiver VCO (TR1151) is determined manually by CV1108 and electronically by varicap diode D1151, which resonate with a shortened 1/4 wave transmission line. The oscillator tracks 21,4MHz below the receiver channel frequency. Output is taken from the oscillator feedback circuit, at the junction of C1158, C1159 and is applied to g1 of buffer TR1153, a dual-gate MOSFET.

JFET TR1154 is the transmitter VCO, the frequency coverage of which is determined manually by CV1109 and electronically by D1153, and a shortened 1/4 wave transmission line; modulation compensation is provided by D853. Output is taken from the oscillator feedback circuit, at the junction of C1173, C1174 and is applied to g1 of buffer TR1156.

The VCO Tx/Rx line (PLA6) is 'low' for receive, thus switching on TR1152, via TR1155, switching on the receiver VCO. When the transceiver is keyed to transmit, the VCO Tx/Rx line is 'high', switching on TR1155 and hence the transmitter VCO. To maintain frequency stability, a ripple-free power supply must be provided for the VCO, and the supply line from the Analogue PWB is smoothed further by capacitance multiplier network C1183, R1175, TR1158.

Output from the two VCO buffers are combined and applied via C1177 to amplifier TR1159. A Wilkinson Splitter, formed by C1189, L1161, C1190, and L1162, C1191, splits power from TR1159 collector equally to each end of R1181. Signal level at the injection coil L1108 is typically +8dBm, which is suitable for application to the 1st mixer TR1102 and the UHF Transmitter power amplifier input.

A sample signal from TR1157 drain is provided for the Prescaler and is presented at PLA4 via C1181.

The Voltage Translation circuit comprises IC1101 and is powered by the 30V line from PLA13. The latter part of IC1101 controls the set-point and slope for the tuning law; RV1101 alters the slope, RV1102 sets the level. Typical tuning voltage range is 8-20V.

DISPLAY CONSOLE

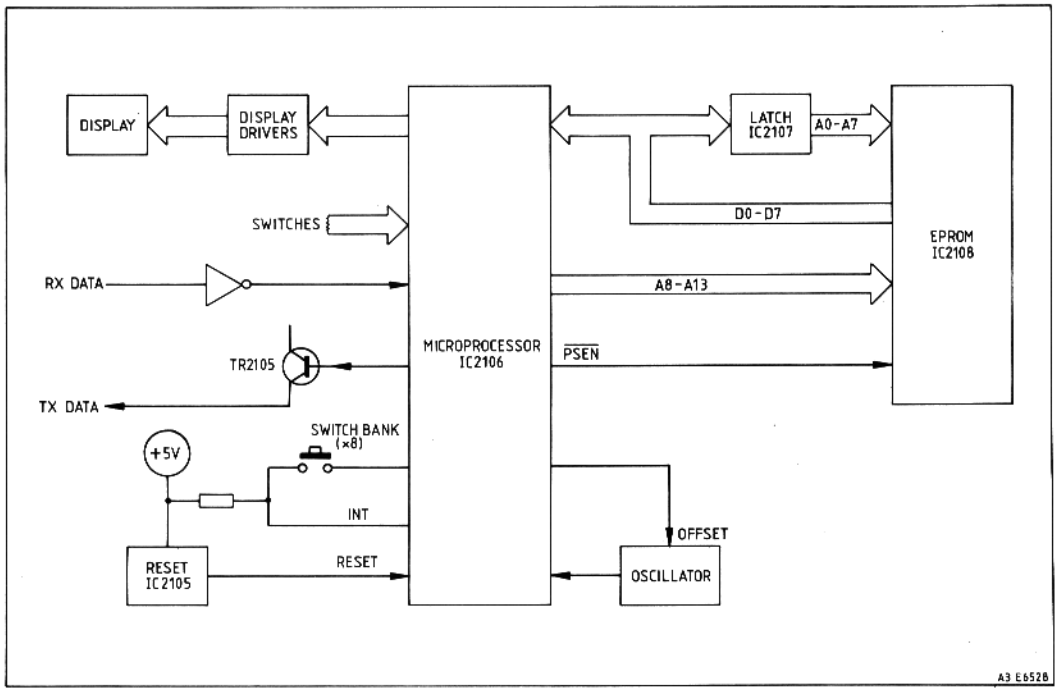


Fig 3.7 Console Block Diagram

Microprocessor IC2106 receives and issues control information to and from peripheral devices. System operation is defined by a set of instructions stored in EPROM IC2108. These instructions are read by the microprocessor by first addressing the EPROM via the 8-bit latch IC2107 and then taking PSEN 'low'. Instructions are read and processed at a speed defined by the microprocessor crystal oscillator frequency and on-board oscillator-dividers. The microprocessor cycles through a loop until an 'interrupt' signal is received.

The microprocessor is reset at pin 10 by Reset chip IC2105 whenever the +5V regulated line drops below an acceptable level. The Console PWB has its own +5V regulator IC2104, which receives power from the transceiver 13,6V line at PLA1.

Two interrupt inputs to the microprocessor, INT0 and INT1, are held at +5V by R2105 and R2104 respectively. When a display button key is depressed, a 'low' is applied to the relevant input to inform the microprocessor to look for key switch action. Switches SW2102-SW2105 put an interrupt on IC2106 pin 14 (INT0) and switches SW2106-SW2109 put an interrupt on IC2106 pin 15 (INT1).

The microprocessor receives data from the transceiver which informs it as to whether clock offset is required for the current channel or not. If offset is required, the microprocessor puts a 'low' on TR2103 base via bridge R2116/R2115. This switches off TR2103 which in turn switches on TR2102, effectively putting C2117 in parallel with C2116 and pulling XL2117 down onto its calibration frequency. The frequency offset is not sufficient to disrupt the operation or timing of the microprocessor (see 'Control PWB').

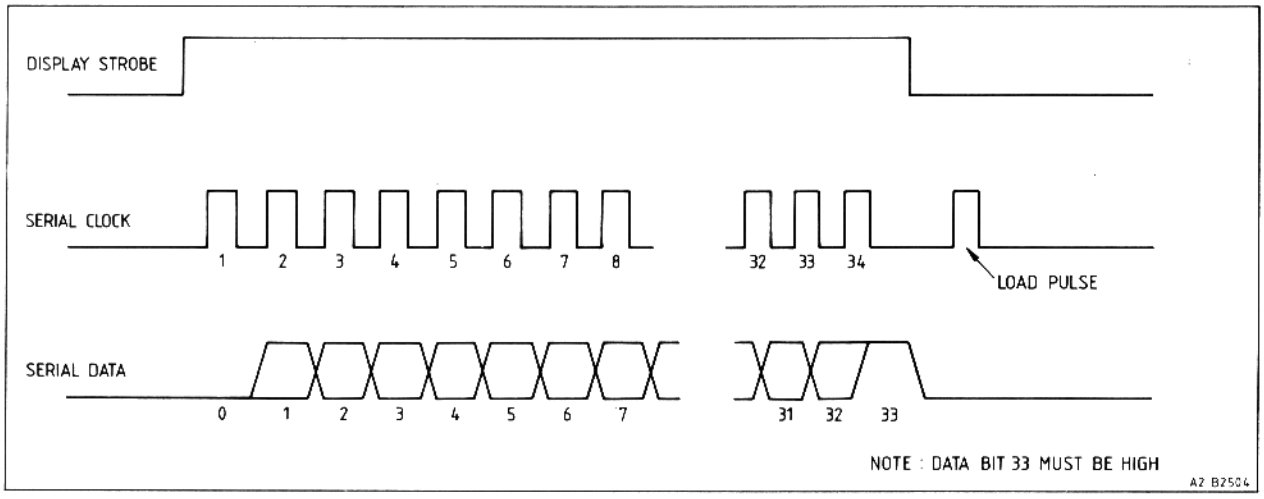


Fig 3.8 Display Driver Timing Diagram

For correct operation, LCD2101 requires a square-wave of approximately 50Hz which is applied to the LCD common backplane, with individual display segments driven in phase to switch them off, or out of phase to switch them on.

Two display drivers IC2101 and IC2102 are employed: these have a three line serial bus structure enabling serial data transfer from IC2106. Both have on-board oscillators; only that in IC2102 is used to drive the LCD backplane, the oscillator in IC2101 is disabled by grounding pin 3.

When the microprocessor makes the DISPLAY STROBE line high, data from the microprocessor is clocked into the driver by SERIAL CLOCK pulses, also provided by the microprocessor. Data is locked into the driver when the DISPLAY STROBE is low. At the 35th clock pulse the data is transferred to the LCD; LCD segments are switched on as a result of corresponding 'high' serial data bits. As data is locked into the driver, the display is updated only when display information needs to be changed, ie as a result of pressing a console button.

The display backlight is switched on and off by the microprocessor via IC2103a,b,c, and TR2104.

Basic Console

The Basic Console comprises principally of IC2006, a parallel-output shift register with a second shift register (IC2004) connected to its serial output. Serial data, clock and strobe lines to the Basic Console are buffered by IC2005. The Data line is normally held high by R2017.

A 2 byte serial message from the Control PWB is transmitted to the Basic Console along the data line and is clocked into the Shift Registers IC2006 and IC2004 respectively. The first serial byte resides in IC2004 and the second in IC2006. If the bit to appear at O7 of IC2006 (pin 12) is set high when the first strobe input to the Basic Console is pulsed high, O7 output will be latched high. (Normally the output is low due to the resistor R2105 pulling the tri-state output down.) This action pulses the strobe input of IC2004, causing the byte residing there to be latched to outputs O0 to O7. Parallel outputs O0 to O6 drive LED indicators via NAND gates IC2002, IC2003. Output O7 drives LED2001 via TR2001.

Input shift register IC2007 may be activated by a strobe from IC2006. The serial input of IC2007 (pin 10) is connected to 0V. While IC2007 remains unstrobed, the inversion and tri-state output of IC2003 result in no data being impressed on the data line when IC2007 receives clock pulses. However, a 'low' on IC2007 pin 1 will prompt it to load parallel data from the console switches into its shift register. This occurs when IC2006 is strobed by a pulse on the strobe line and the byte held in its shift register results in a low level at O6. If, at this moment, any of the switches SW2002 to SW2008 are closed, the serial output byte shifted out of IC2007 (by the next eight clock pulses) will contain low levels at the relevant switch positions. IC2007 serial output is OR'ed to the data line by a section of NAND gate IC2003. The data line can then be read by the Control PWB.

Power on indication is provided by LP2001 switched in parallel with the ON/OFF line by a section of SW2001. A regulated 5V supply is provided by IC2001. Potentiometer RV2001 is the voltage control for the loudspeaker volume.

Standard Microphone AT29036

An electret microphone insert with integral FET amplifier is used, and receives a nominal 4,7V power supply produced by zener diode D1501, derived from the transceiver's nominal +13,6V supply (via R1501). Microphone output is presented at PLA5.

Hookswitch SW1503 is a reed switch which closes when it is in the proximity of a magnetic field, normally when the microphone is located within the microphone rest ("On Hook"). Facility switch SW1502 may be used instead of one of the Console keys, subject to transceiver programming.

Basic Console

Remove the console from the transceiver or cradle, depending on installation. Unscrew the two self-tapping screws securing the backplate (121) to the front panel (126). Remove the volume control knob (124) and pull the front panel off its spindle. To remove the PWB, undo the two M2,5 screws securing it to the backplate. Access to components is gained by removing two screws which secure the reflector support (129) to the PWB.

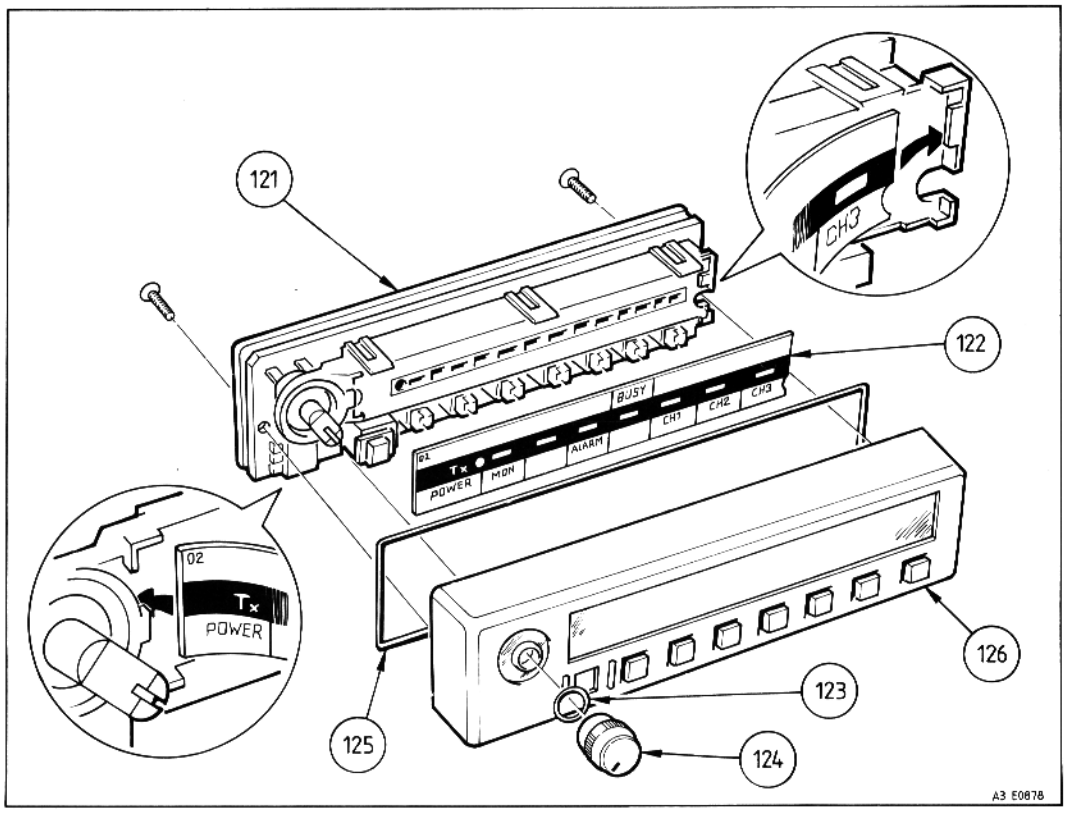


Fig 4.4A Basic Console Assembly

Re-assembly is the reverse of disassembly, but ensure that the small rubber 'O'-Ring (123) is not dislodged by the volume control spindle when fitting the front panel over the PWB/Backplate assembly. Finally, ensure that the gasket (125) is seated correctly round the backplate.

The Graphics Panel is tucked under two lugs at opposing ends of the light-pipe.

CHANGE OF CHANNEL FREQUENCIES

Note: The following checks should be carried out when changing the transceiver channel frequencies to ensure that birdies (internally generated spurii) are not present on any programmed channel.

On change of equipment channel frequencies, it may be necessary to change the reference oscillator and 2nd oscillator crystals (in addition to the EPROM). Receiver channels near harmonics of 12MHz may require Microprocessor Offset to be enabled (see Appendix A).

Transmitter and receiver re-alignment should not be necessary.

CRYSTAL INFORMATION

Receiver 2nd oscillator

Standard Frequency	20,945MHz (Part No 4313 320 90021)
Alternative Frequency	21,855MHz (Part No 4313 320 90031)
Specification:	E312
Temperature Range:	-30°C to +60°C
Freq/Temp Tolerance:	±15ppm (+25°C ref)

The alternative crystal frequency is only used when the receiver carrier frequency lies within the following bands:-

83,680 - 83,880MHz	418,800 - 419,000MHz
146,575 - 146,775MHz	439,745 - 439,945MHz
167,460 - 167,660MHz	460,690 - 460,890MHz
188,505 - 188,705MHz	481,635 - 481,905MHz
209,350 - 209,550MHz	502,580 - 502,780MHz

The Comprehensive Data Programmer (CDP) calculates the required crystal frequency during the FM1000 validation routine and issues a message indicating which crystal is required.

Approved Suppliers: Toyocom, ITT (UK), Hy-Q.

Synthesiser Reference Oscillator

	Freq/Temp Tolerance (+25°C Ref)	
	±5ppm	**±2ppm**
Standard (8,4MHz):	3513 505 01461	3513 500 00601
Alternative (7,2MHz):	3513 505 01441	3513 500 00581
Alternative (7,8MHz):	3513 505 01451	3513 500 00591
Alternative (9,0MHz):	3513 505 01471	3513 500 00611
Specification:	P325	
Temperature Range:	-10°C to +70°C	-30°C to +70°C

The CDP calculates the required crystal frequency during the FM1000 validation routine and issues a message indicating which crystal is required.

Any subsequent changes or additions made to receiver channel frequencies must be checked for birdies (harmonics of reference oscillator). If any birdies are present, a new reference oscillator frequency must be calculated (for zero or minimum number of birdies) starting with 8,4MHz as the preferred option and then working through the alternatives specified. Once the most suitable reference oscillator has been determined and fitted, ALL receiver channels must be re-checked for birdies.

Approved Suppliers for ±5ppm crystals: Toyocom, ITT (UK), Hy-Q.

High stability (±2ppm) Reference Oscillator modules are available direct from Philips RCS.

TEST MODE

To align the radio, it is neccessary to override its signalling protocol. This is achieved by setting it into test mode.

To select test mode, switch off the radio and then connect pin 6 of the Battery Lead Assembly to pin 4 (0V).

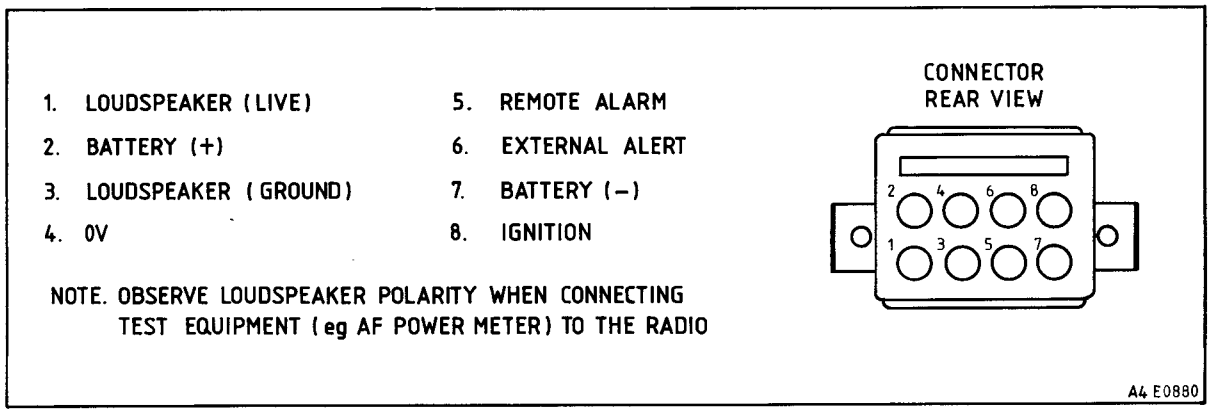


Fig 4.2 Battery Lead Connector

On selection of test mode, FM1200 radios tune to the Base Channel (Channel 0). In order to fully align the radio it will be necessary to select channels at the lower, middle and upper ends of the frequency band of the radio. The radio calculates its receiver and transmitter channels from a synthesiser base code. In order to select other frequencies this code must be changed. Note that it is only possible to select alignment channels in Test Mode.

Table 4.1 - Synthesiser Codes for Test Frequencies (FM1200 only)

Freq (MHz)	Code	Freq (MHz)	Code
68	10880	225	36000
75	12000	400	16000
78	12480	410	17600
88	14080	420	19200
132	21120	425	20000
138	22080	431	20960
144	23040	437	21920
146	23360	440	22400
153	24480	447	23520
156	24960	450	24000
160	25600	455	24800
174	27840	470	27200
183	29280	482	29120
192	30720	495	31200
200	32000	520	35200
208	33280		

On selection of test mode, FM1300 radios tune to Channel 1. Low, mid and high alignment channel frequencies are stored in EEPROM and reference to the Equipment Data Sheet should be made to identify these.

KEYPAD CONSOLES (FM1200 only)

Receiver and Transmitter Frequencies

By "dialling-in" certain number strings via the Keypad Console it is possible to alter the transmitter and receiver codes.

Overwrite Tx Test Base Code:

Enter "202nnnnn #" where "nnnnn" is the new Tx Test Base Code number.

For Example;

to change the base code to 192MHz (code 30720), type "20230720" followed by "#".

Overwrite Rx Test Base Code:

Enter "201nnnnn #" where "nnnnn" is the new Rx Test Base Code number.

The radio will only respond to new base codes if a valid receiver base code is entered. If a transmitter base code only is entered, the radio will ignore this code and use the existing code. This does not preclude entering the existing receiver base code with a new transmitter code.

FFSK Signalling

The dialled strings used to control the FFSK encoder can be dialled directly from the console keypad, as follows:-

Enter "30000001#"	to transmit a 1200Hz tone.
Enter "30000002#"	to transmit a 1800Hz tone.
Enter "30000003#"	to encode 101.. sequence.
Enter "30000000#"	to disable tone output.

TEST DATA (FM1200 only)

Calculation of Tx & Rx Synthesiser base codes

$$\text{Synthesiser Base Code} = \frac{\text{Channel Frequency - Base Frequency}}{\text{Reference Frequency}}$$

where:- Base Frequency = 0MHz for VHF and 300MHz for UHF Bands.

Reference Frequency

6,25kHz or 5,0kHz (depending on channel spacing)

ALIGNMENT PROCEDURE

Notes: 1. Transmitter Alignment MUST be carried out before aligning the receiver.

2. The majority of alignment is carried out at PWB level before fitting to the transceiver, and should not need to be repeated during equipment alignment. Hence such alignment stages have been omitted from the following procedures.

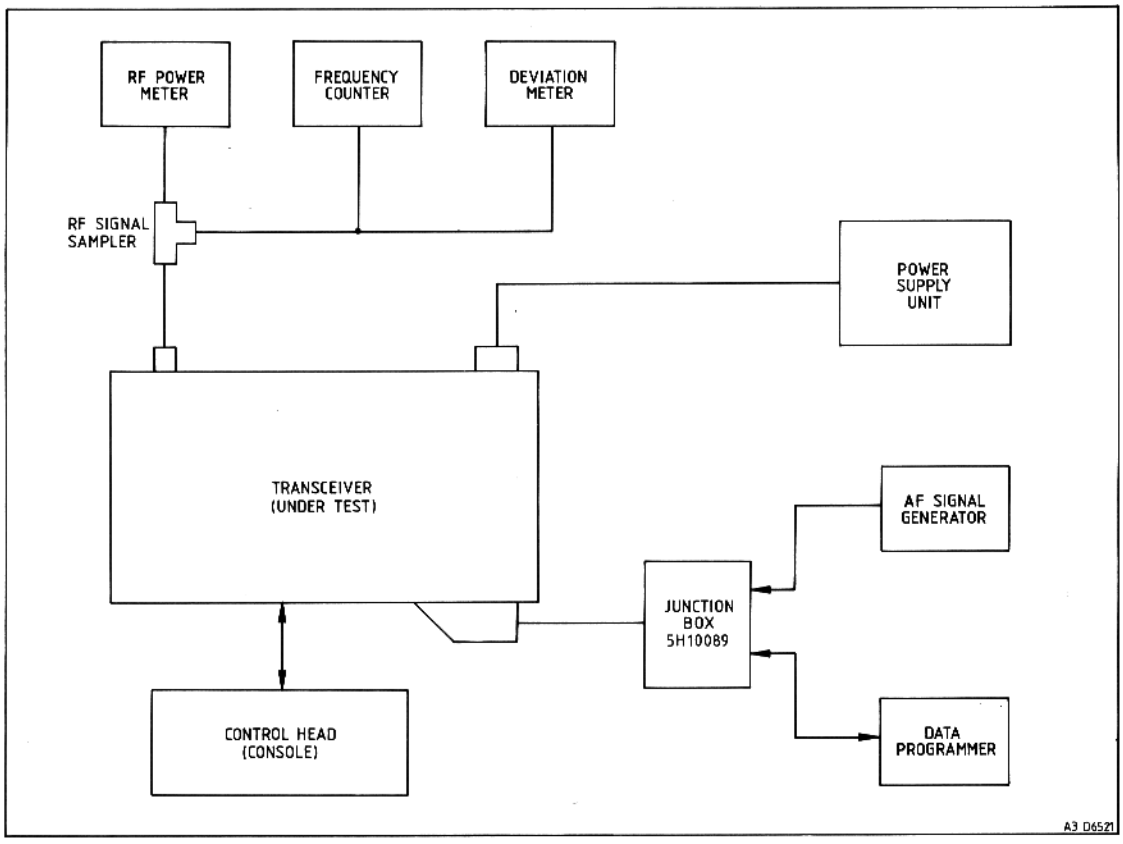


Fig 4.5 Synthesiser and Transmitter Test Connections

Note: Before commencing alignment, remove the 5-way Power Connector (PLB) from the Tx PA module before applying DC Power to the equipment.

Synthesiser

	TUNE	*ACTION*
1.	RV301	Adjust to give 30V ±0,2V at PLF 7 on the Analogue PWB.

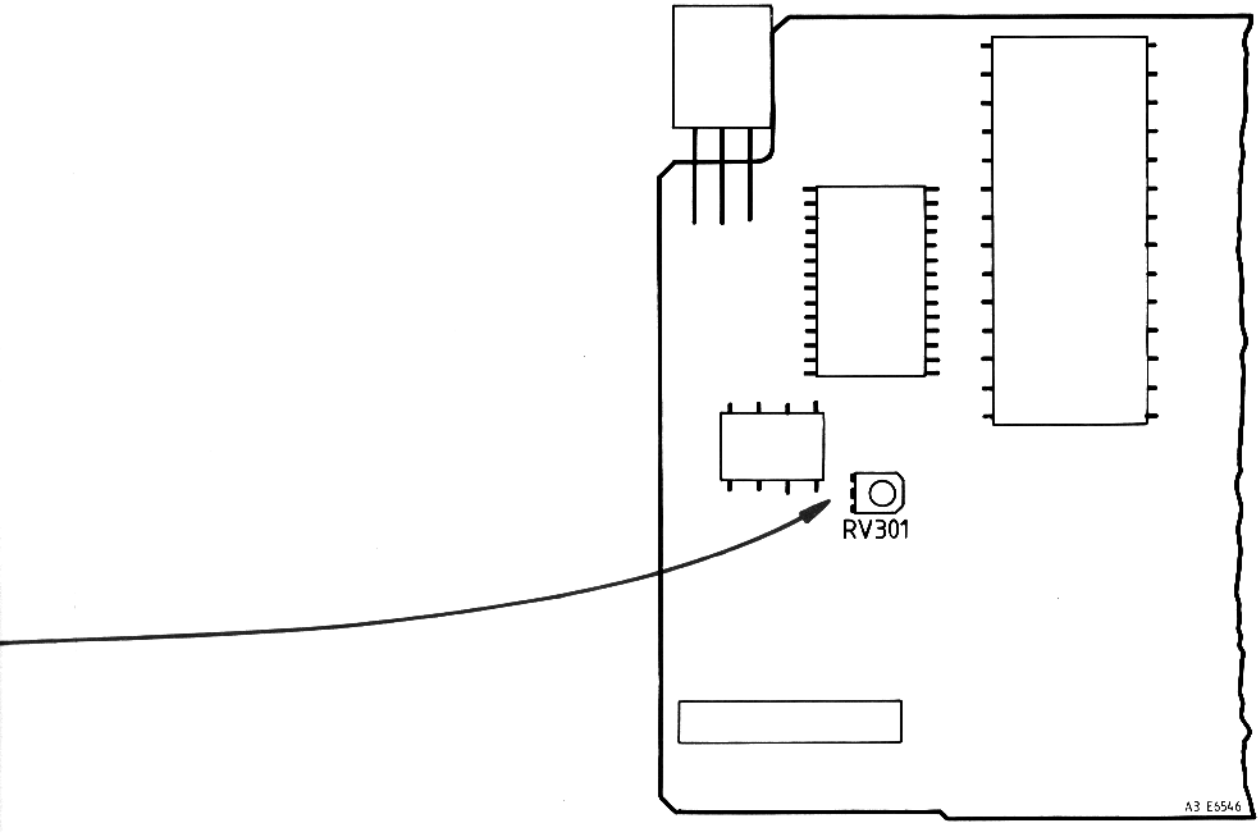

RV301
A3 E5546

Table 4.1

Frequency Band/Calibration Frequency								
E0	B0	A9	K1	K2	U0	TM	T4	WM
76MHz	144MHz	160MHz	176MHz	208MHz	455MHz	420MHz	437MHz	495MHz

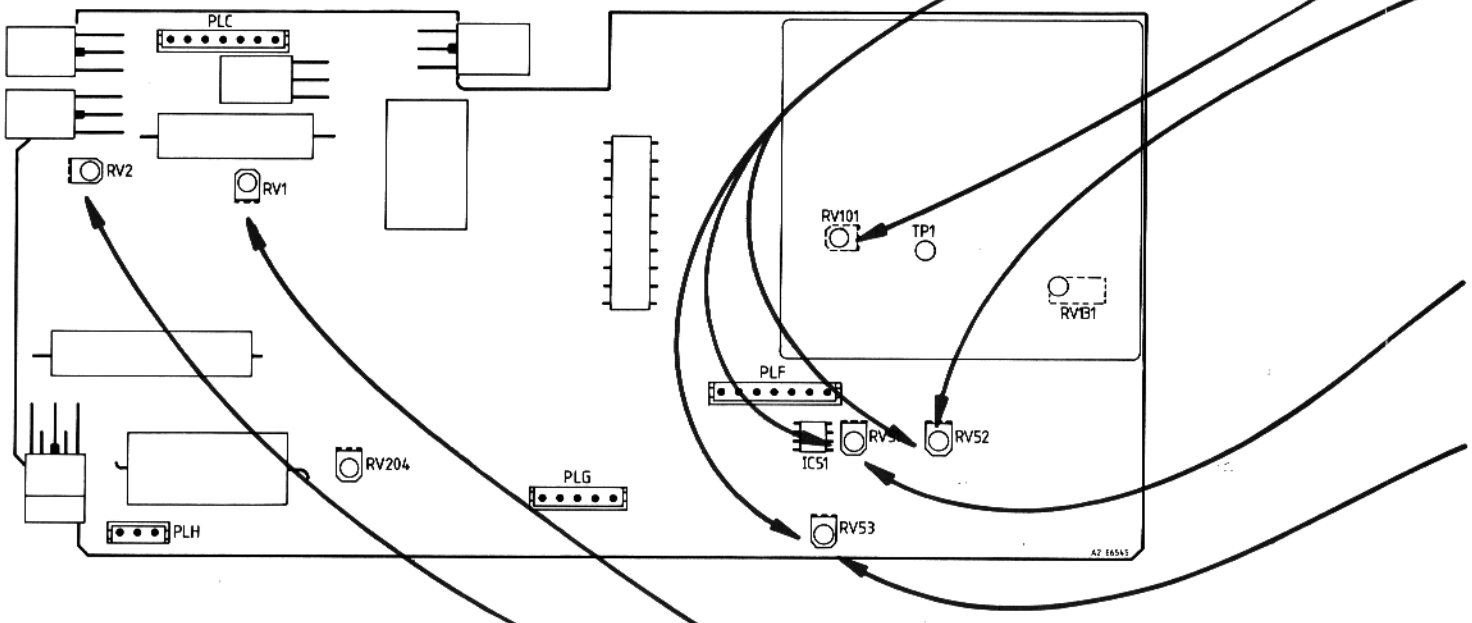


Fig 4.7 Modulation and Transmitter Alignment Diagram

Table 4.2

Code	Function
RV1	Set Power
RV2	Limit Volts
RV51	Modulation Balance
RV52	Peak Deviation
RV53	Microphone Gain
RV101	Phase Comparator Gain

Modulat

TUNI

1.

2. RV5
RV53

3. RV1C

4. RV52

5. RV51

6.

7. RV53

8.

Transmit

Note

TUNE

1.

2. RV2

3.

4. RV1

Modulation

	TUNE	*ACTION*
1.		Using the PDP, set the transmitter to the appropriate calibration frequency in Table 4.1 (left). Use a non-customized channel (eg "#102.00") if possible.
2.	RV51, RV52 RV53	Set fully anticlockwise. Tune AF signal generator to 1kHz and adjust output level to produce a peak deviation level of ±3kHz (±100Hz).
3.	RV101	Adjust to produce 60mV peak-to-peak at TP1.
4.	RV52	With the AF signal generator set to 1kHz at an output level of 30mV RMS, adjust (peak deviation) to 90% peak system deviation as shown below:-

Channel Spacing	Deviation Level
25kHz (V)	±4,0kHz
20kHz (R)	±3,25kHz
12,5kHz (S)	±2,0kHz

5.	RV51	Adjust (mod balance) to give minimum ripple voltage at TP1.
6.		Repeat steps (6) and (7) until interaction between adjustments ceases.
7.	RV53	With AF signal generator level reduced to 3mV RMS, adjust to give 60% peak system deviation.
8.		Using the portable data programmer, erase the test frequency, or lock it out.

Transmitter Power Control

Note: Key the transmitter for the minimum time required to make the relevant reading or adjustment.

	TUNE	*ACTION*
1.		Refit 5-way connector PLB to the Tx PA. Using the PDP, set the transmitter to the maximum power level (#104.2 for Low Power UHF, #104.5 for K1/K2, #104.6 for all others) and calibration frequency for the equipment frequency band (see Table 4.3).
2.	RV2	Adjust to give the "limit volts" reading (as shown in Table 4.3) at PLC pin 6.
3.		Set transmitter power to 25W (#104.5), or 6W (#104.2) for low power UHF versions.
4.	RV1	Adjust RV1 for 25W (6W for low-power UHF) reading on the power meter.

TUNE	ACTION
5.	Using the PDP, reset the transmitter power parameter to that required by the user. Key on the transmitter and check that the correct power output is achieved (to within ±1,5dB).
6.	Using the portable data programmer, erase the calibration frequency, or lock it out.

Table 4.3

Frequency Band	Calibration Frequency	Calibration Power 0,5W	Limit Volts 0,1V
E0 68 - 88MHz	76MHz	25W	10V
B0 132 - 156MHz	138MHz	25W	11V
A9 146 - 174MHz	153MHz	25W	11V
K1 174 - 208MHz	183MHz	25W	11V
K2 192 - 225MHz	200MHz	25W	11V
TM 425 - 450MHz Low Power	410MHz	6W	9V
TM 425 - 450MHz High Power	410MHz	25W	9V
T4 425 - 450MHz Low Power	430MHz	6W	9V
T4 425 - 450MHz High Power	430MHz	25W	9V
U0 440 - 470MHz Low Power	450MHz	6W	9V
U0 440 - 470MHz High Power	450MHz	25W	9V
WM 470 - 520MHz Low Power	490MHz	6W	9V
WM 470 - 520MHz High Power	490MHz	25W	9V

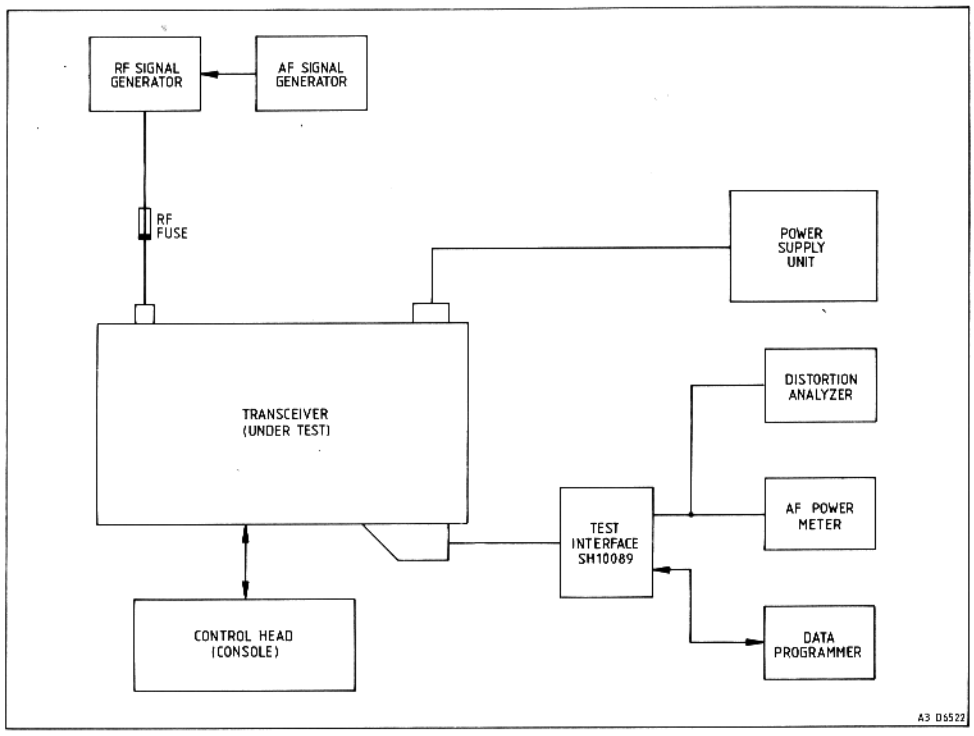


Fig 4.8 Receiver Test Connections

	TUNE	ACTION
1.		Adjust the RF signal generator output to give 12dB SINAD.
2.	RV204	Adjust to give a reading of 4,0V DC (±0,1V) at PLB pin 1.

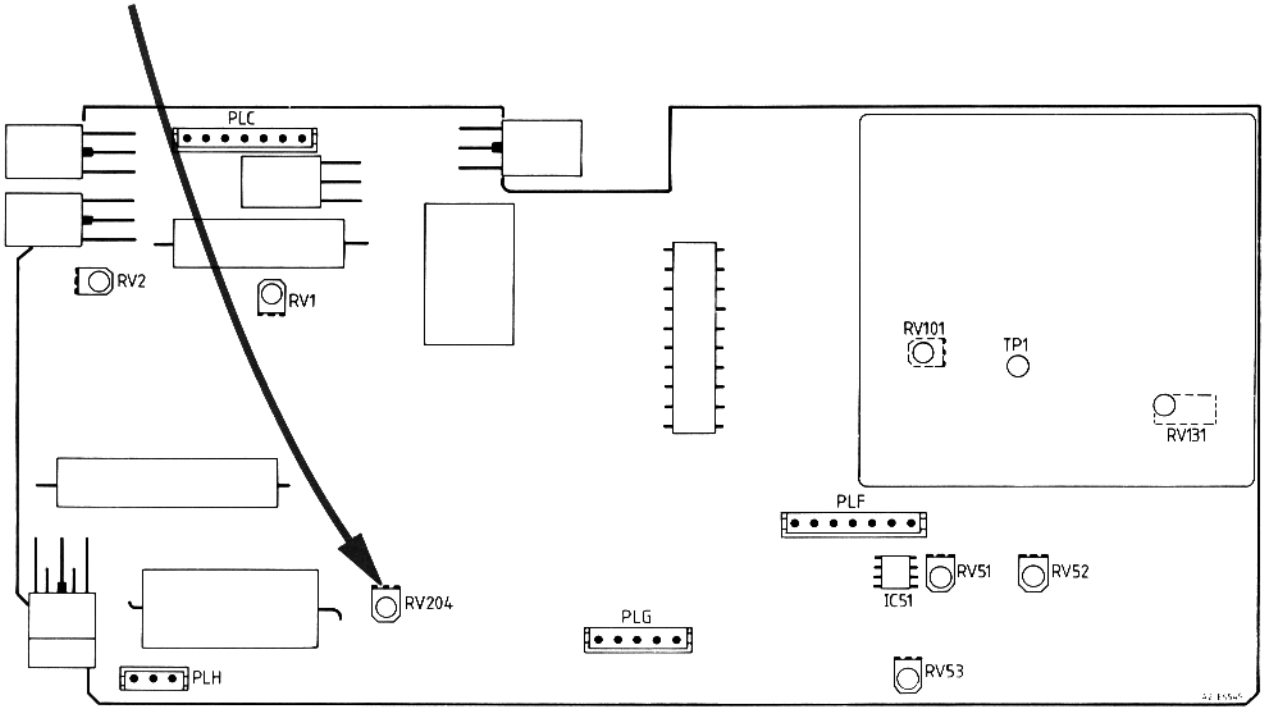


Fig 4.9 Receiver Alignment Diagram

PERFORMANCE CHECKS

Preliminaries

1. Interface between test equipment and transceiver is to be made via the facility connector.

2. Transceiver is to have covers fitted.

Transmitter

1. RF Power

Check that the RF power output on those channels with the lowest, mid and highest frequencies, is as follows:-

	E0,B0,A9	K1,K2	U,T,W, Low Pwr	U,T,W, High Pwr
(a) Nominal RF power @ 13,6V	30W	25W	7W	25W
Maximum current	<7A	<7A	<3,5A	<8A
Minimum current	>4,5A	>4,5A	>2A	>5A
RF Power @ 10,8V	>20W	>15W	>4W	>15W
RF Power @ 15,6V	<35W	<30W	<8W	<30W
(b) RF Power adjustment	1-30W	1-25W	1-7W	2,5-25W
Max power to which equipment should be adjusted	35W	30W	10W	30W
Power variation across frequency band	1dB	1dB	1dB	1dB

2. Peak System Deviation

Adjust AF generator to give 60% peak system deviation at 1kHz. Increase output level by 20dB and check that the following peak system deviation is within the limits specified for the lowest and highest channel frequencies.

Channel Spacing	Deviation Limits
25kHz (V)	±4,0kHz to ±5,0kHz
20kHz (R)	±3,2kHz to ±4,0kHz
12,5kHz (S)	±2,0kHz to ±2,5kHz

3. Microphone Amplifier

Set the AF signal generator output to 1kHz at a level of 3mV RMS and check that between 50%-70% peak system deviation is obtained.

4. Modulation Distortion

Adjust the AF signal generator output to produce 60% peak system deviation at 1kHz and check that the distortion level is not greater than 2%.

5. Frequency Error

Check that the RF carrier frequency is within ±5ppm (standard) or ±2,5ppm (option) of any channel centre frequency.

Receiver

1. Rated Audio Output

With an RF input of 1mV PD, modulated by 1kHz at 60% peak system deviation, check that the AF output is not less than 3W at less than 5% distortion into a 3Ω load.

2. Reference Sensitivity

With an RF input modulated by 1kHz at 60% peak system deviation, adjust the volume control for 1,5W AF output. Adjust the RF level to produce 12dB SINAD and check that the level is less than 0,31µV PD. Note that signal generator calibration is rarely better than ±2dB.

3. Limiting Characteristics

Less than 2dB change in audio output with RF input change from 0,5µ230 PD to 100mV PD.

4. IF Bandwidth (Nose)

Set the RF signal generator output level to +6dB wrt the level required to produce 20dB noise quieting. Tune the RF frequency above and below the centre frequency to obtain 20dB quieting and check that it is obtained with the following frequency adjustments:-

25kHz	(V) sets	greater than ±7,0kHz
20kHz	(R) sets	greater than ±6,0kHz
12,5kHz	(S) sets	greater than ±3,75kHz

5. IF Bandwidth (Skirt)

Set the RF signal generator output level to +90dB wrt 0,5µ230V PD. Check that the quieting level is below 20dB at the appropriate frequency displacements stated below:-

25kHz	(V) sets	less than ±25kHz
20kHz	(R) sets	less than ±20kHz
12,5kHz	(S) sets	less than ±12,5kHz

6. Squelch Threshold, Opening and Closing Level

Adjust the RF signal generator output to level required to give the programmed squelch opening level (9, 12, 15, 18, 21 or 24dB SINAD) and check that the squelch opens. Reduce generator output to that level required to produce 9dB SINAD and check that the squelch closes.

7. Residual Noise

Set the volume control to maximum and with squelch closed, check that the AF millivoltmeter reading is less than 10mV.

8. Audio Sensitivity

Set the volume control to maximum. Set the RF signal generator output level to 1mV PD and modulate with 1kHz tone. Check that the tone deviation level required to produce a AF power reading of 3W is less than 40% peak system deviation.

9. Maximum Current

Check the transceiver current readings with the following test conditions:-

Receiver squelched, no RF signal	less than 700mA
RF input of 1mV PD modulation frequency 1kHz at 60% peak system deviation and volume control set for 3W AF output	less than 1,1A

STANDARD MICROPHONE

Grey **Part No 3513 505 00691**
Brown **Part No 3513 505 00121**

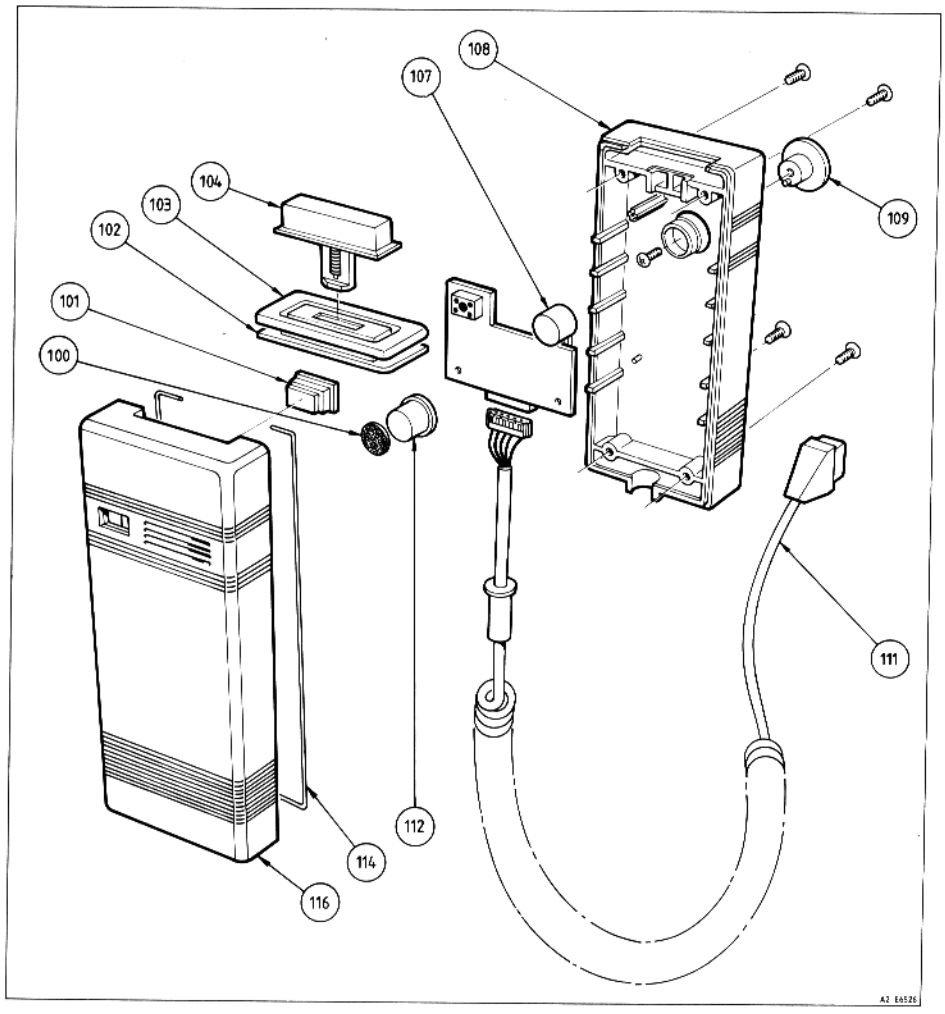
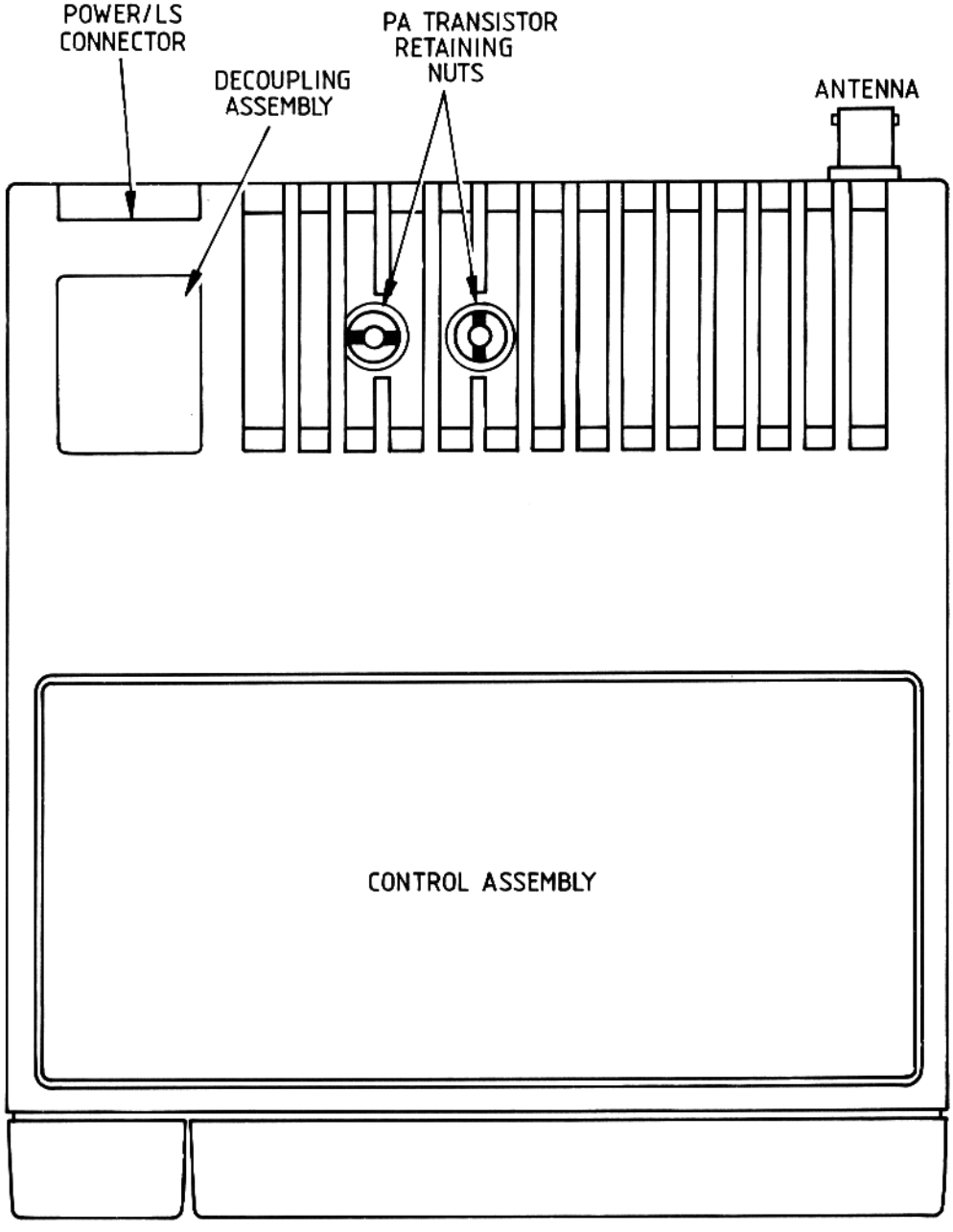


Fig 5.5 Exploded Diagram - Standard Microphone

Item No	Description	Grey	Brown
(100)	Disc, Acoustic	3513 901 50001	3513 901 50001
(101)	Facility Key	3513 903 00071	3513 903 00021
(102)	Seal (1/Pressel)	3513 905 80061	3513 905 80061
(103)	Support Ring (1/Pressel Seal)	3513 905 60011	3513 905 60011
(104)	Pressel (requires Spring 3513 905 80101)	3513 904 50151	3513 904 50161
(107)	Microphone, Electret	4313 322 90001	4313 322 90001
(108)	Case Back	3513 900 90051	3513 900 90031
(109)	Knob, Mic Rest (1/Case Back)	3513 903 00061	3513 903 00041
(111)	Plug Assembly, Data, 5-way	3513 505 00051	3513 505 00571
(112)	Housing, Support (1/electret insert)	3513 902 30031	3513 902 30031
(114)	Silicon Rubber Seal	3513 905 80111	3513 905 80111
(116)	Case Front	3513 900 90041	3513 900 90011


POWER/LS
CONNECTOR
DECOUPLING
ASSEMBLY
PA TRANSISTOR
RETAINING
NUTS
ANTENNA
CONTROL ASSEMBLY

FIG

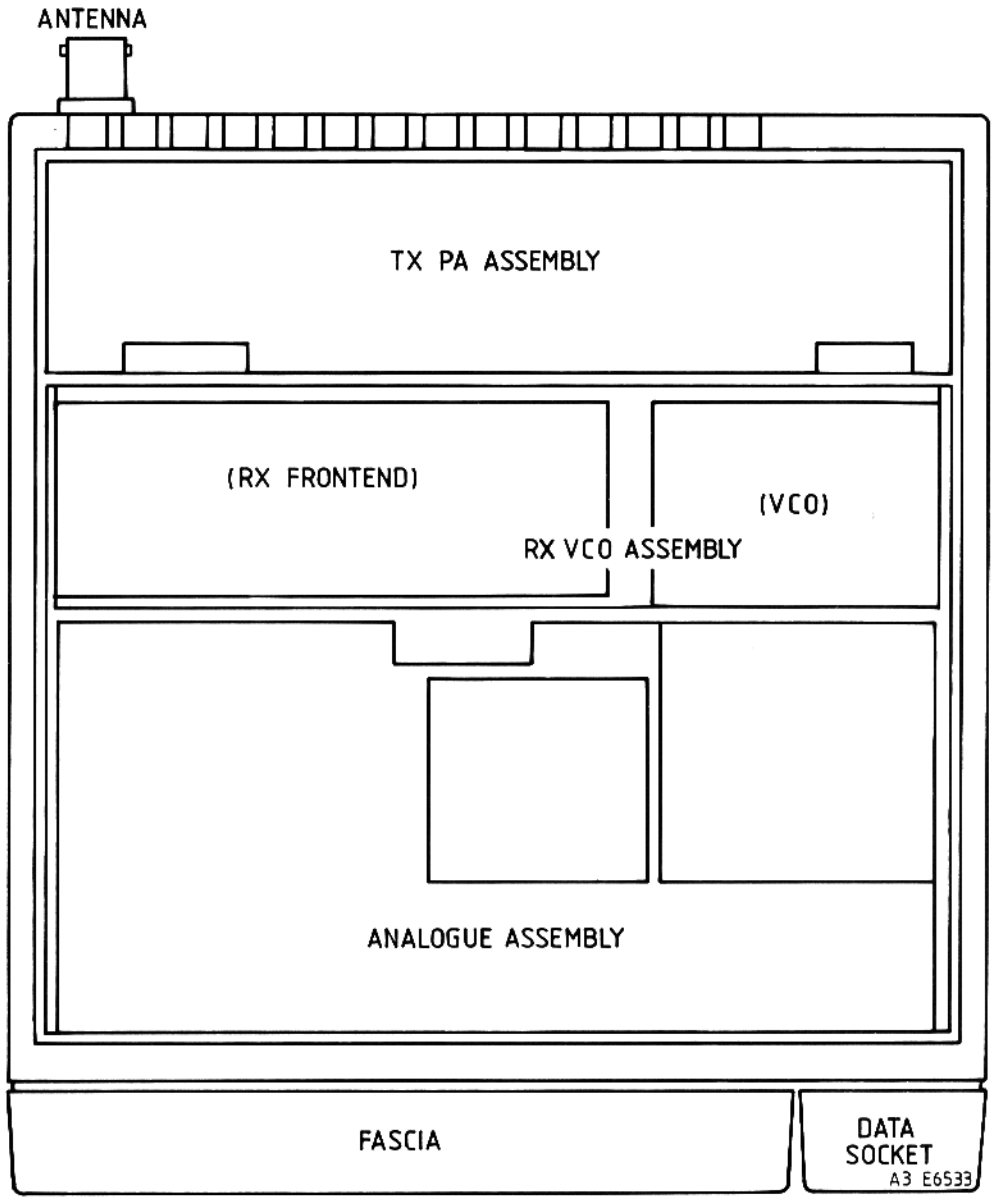


FIG 6.1 TRANSCEIVER LAYOUT DIAGRAM

TP253

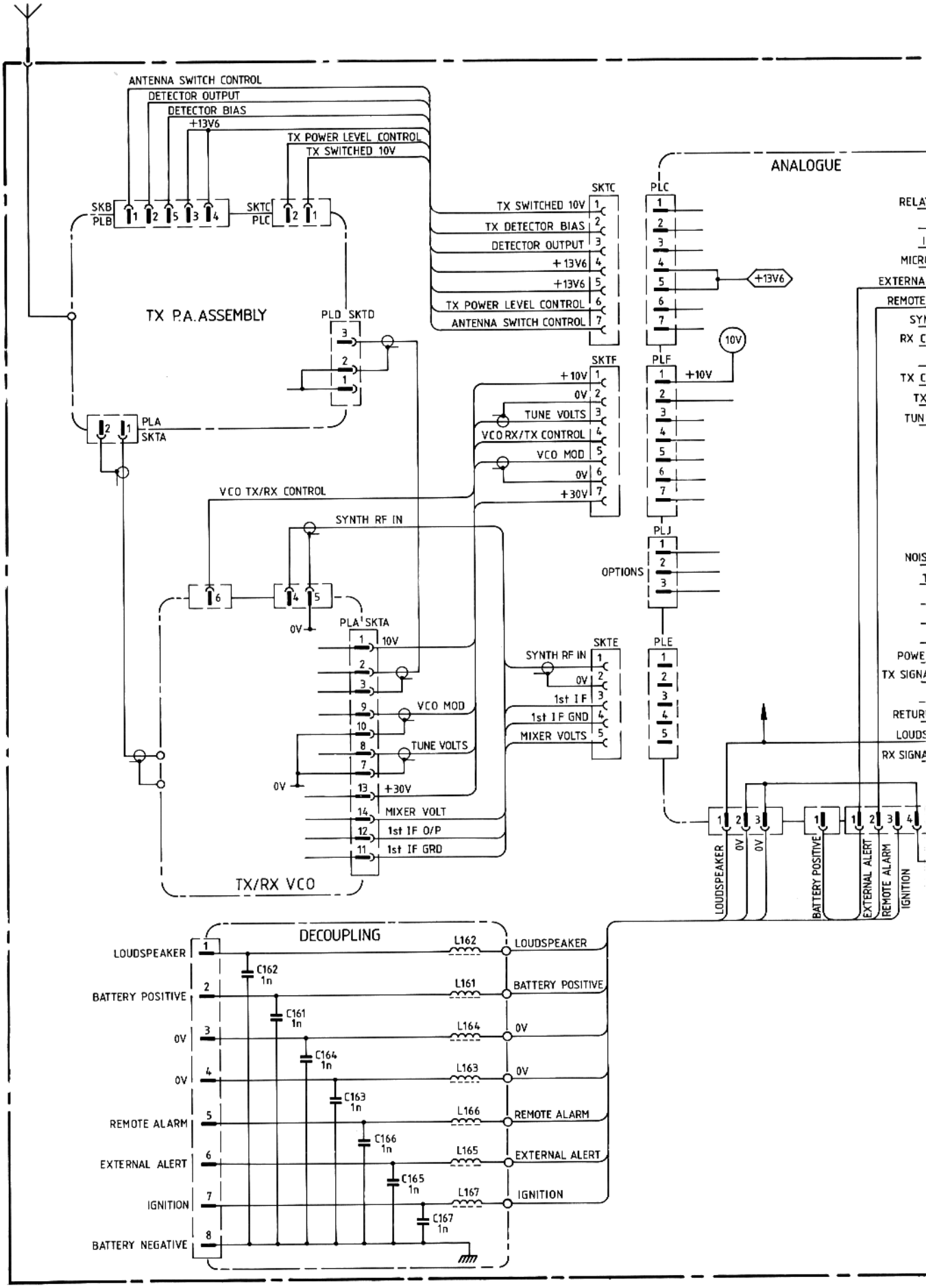
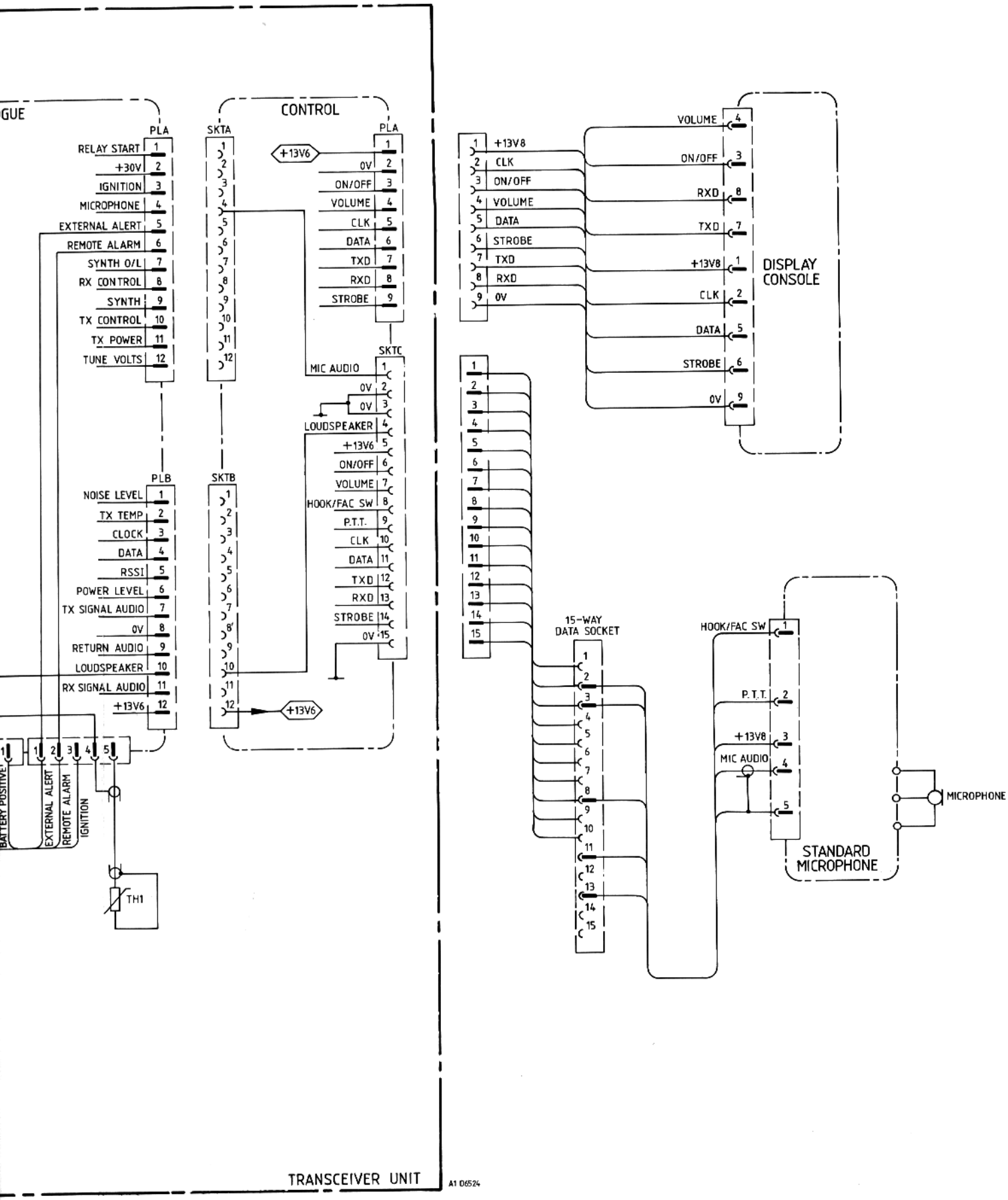
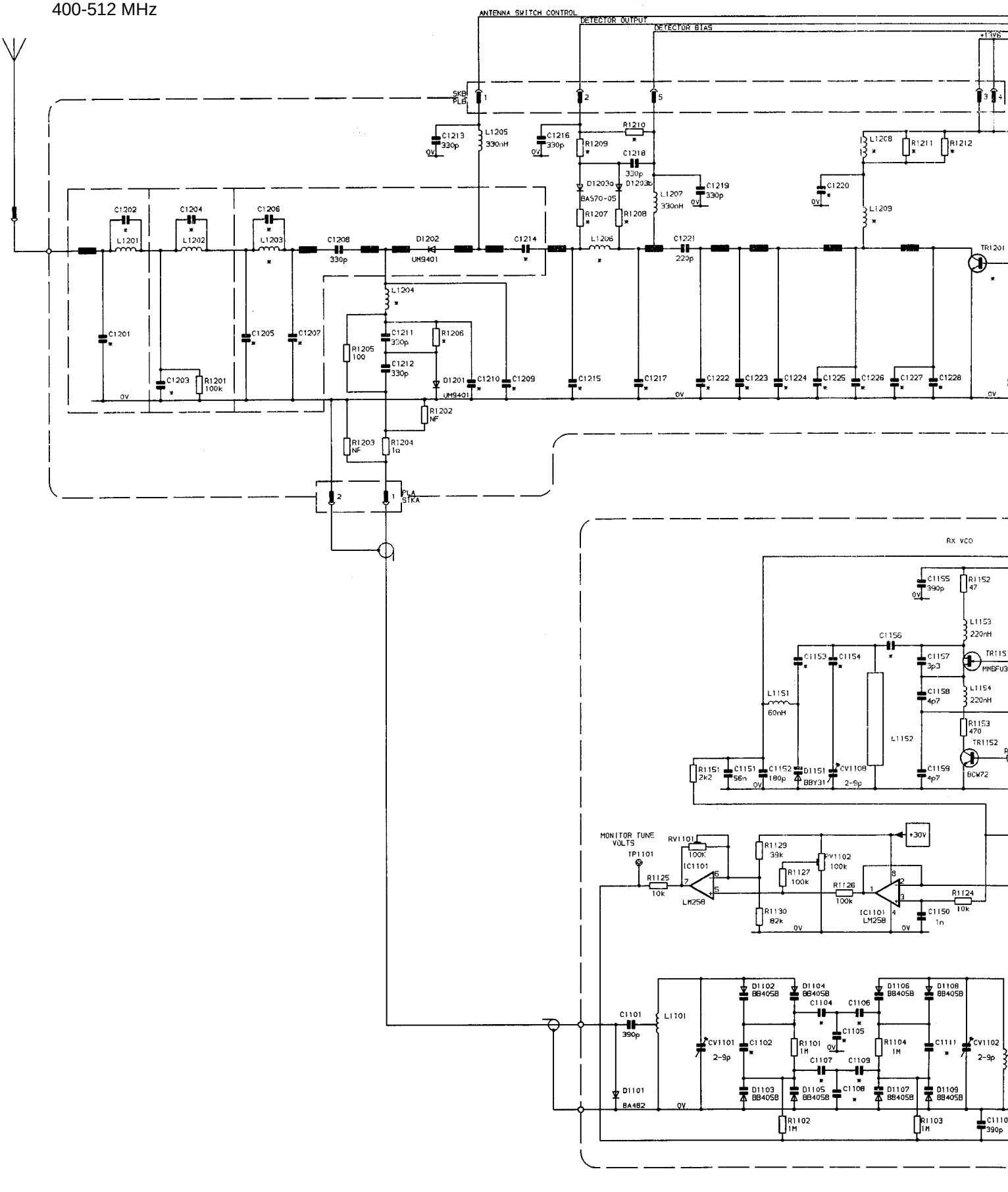


FIG 6.2 TRANSCEIVER INTERCONNECTION DIAGRAM


GUE
PLA
RELAY START 1
+30V 2
IGNITION 3
MICROPHONE 4
EXTERNAL ALERT 5
REMOTE ALARM 6
SYNTH O/L 7
RX CONTROL 8
SYNTH 9
TX CONTROL 10
TX POWER 11
TUNE VOLTS 12
PLB
NOISE LEVEL 1
TX TEMP 2
CLOCK 3
DATA 4
RSSI 5
POWER LEVEL 6
TX SIGNAL AUDIO 7
0V 8
RETURN AUDIO 9
LOUDSPEAKER 10
RX SIGNAL AUDIO 11
+13V6 12
BATTERY POSITIVE
EXTERNAL ALERT
REMOTE ALARM
IGNITION
TH1
CONTROL
SKTA
PLA
+13V6
0V 2
ON/OFF 3
VOLUME 4
CLK 5
DATA 6
TXD 7
RXD 8
STROBE 9
SKTC
MIC AUDIO 1
0V 2
0V 3
LOUDSPEAKER 4
+13V6 5
ON/OFF 6
VOLUME 7
HOOK/FAC SW 8
P.T.T. 9
CLK 10
DATA 11
TXD 12
RXD 13
STROBE 14
0V 15
SKTB
+13V6
TRANSCEIVER UNIT
A1 06524
+13V8 1
CLK 2
ON/OFF 3
VOLUME 4
DATA 5
STROBE 6
TXD 7
RXD 8
0V 9
VOLUME 4
ON/OFF 3
RXD 8
TXD 7
+13V8 1
CLK 2
DATA 5
STROBE 6
0V 9
DISPLAY CONSOLE
15-WAY DATA SOCKET
HOOK/FAC SW 1
P.T.T. 2
+13V8 3
MIC AUDIO 4
5
MICROPHONE
STANDARD MICROPHONE

TION

400-512 MHz


ANTENNA SWITCH CONTROL
DETECTOR OUTPUT
DETECTOR BIAS
+13V6
SKB PLB
PLA STKA
RX VCO
MONITOR TUNE VOLTS
+30V
0V
L1205 330nH
L1204
L1201
L1202
L1203
L1206
L1207 330nH
L1208
L1209
L1151 60nH
L1152
L1153 220nH
L1154 220nH
TR1201
TR1151 MMBFU3
TR1152 BCW72
D1202 UM9401
D1201 UM9401
D1203a BA570-05
D1203b
D1101 BA482
D1102 BB405B
D1103 BB405B
D1104 BB405B
D1105 BB405B
D1106 BB405B
D1107 BB405B
D1108 BB405B
D1109 BB405B
D1151 BBY31
IC1101 LM258
RV1101 100K
CV1101 2-9p
CV1102 2-9p
CV1108 2-9p
TP1101
R1201 100k
R1202 NF
R1203 NF
R1204 1Ω
R1205 100
R1206
R1207
R1208
R1209
R1210
R1211
R1212
R1101 1M
R1102 1M
R1103 1M
R1104 1M
R1124 10k
R1125 10k
R1126 100k
R1127 100k
R1129 39k
R1130 82k
R1151 2k2
R1152 47
R1153 470
C1101 390p
C1102
C1104
C1105
C1106
C1107
C1108
C1109
C1110 390p
C1111
C1150 1n
C1151 56n
C1152 180p
C1153
C1154
C1155 390p
C1156
C1157 3p3
C1158 4p7
C1159 4p7
C1201
C1202
C1203
C1204
C1205
C1206
C1207
C1208 330p
C1209
C1210
C1211 330p
C1212 330p
C1213 330p
C1214
C1215
C1216 330p
C1217
C1218 330p
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C1220
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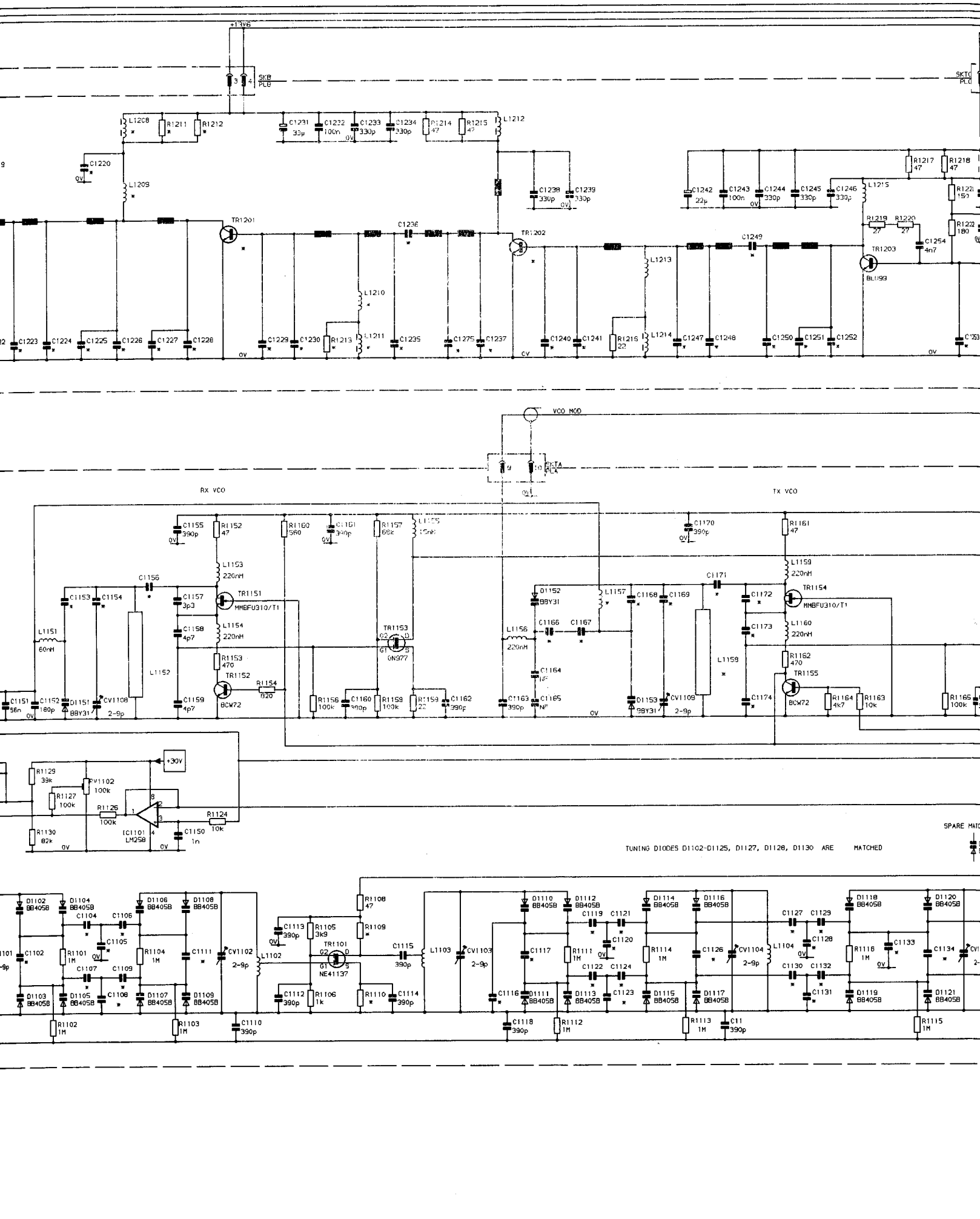
C1222
C1223
C1224
C1225
C1226
C1227
C1228


+13V6
SKB PL8
L1208
R1211
R1212
C1231 33µ
C1232 100n
C1233 330p
C1234 330p
R1214 47
R1215 47
L1212
C1220
L1209
C1238 330p
C1239 330p
R1217 47
R1218 47
C1242 22µ
C1243 100n
C1244 330p
C1245 330p
C1246 330p
L1215
R1219 27
R1220 27
C1254 4n7
TR1203
BLU99
TR1201
TR1202
C1236
C1249
L1213
L1210
L1211
R1213
C1235
C1275
C1237
C1240
C1241
R1216 22
L1214
C1247
C1248
C1250
C1251
C1252
C1223
C1224
C1225
C1226
C1227
C1228
C1229
C1230
0V
VCO MOD
SKTA PL4
Rx VCO
Tx VCO
C1155 390p
R1152 47
R1160 560
C1161 340p
R1157 68k
L1155 15nH
L1153 220nH
C1156
C1153
C1154
C1157 3p3
TR1151 MMBFU310/T1
L1151 60nH
C1158 4p7
L1154 220nH
R1153 470
TR1152 BCW72
R1154 820
L1152
C1151 56n
C1152 180p
D1151 BBY31
CV1108 2-9p
C1159 4p7
R1156 100k
C1160 390p
R1158 100k
R1159 22
C1162 390p
TR1153 ON977
C1170 390p
R1161 47
L1159 220nH
C1171
TR1154 MMBFU310/T1
D1152 BBY31
L1157
C1168
C1169
C1172
L1156 220nH
C1166
C1167
C1173
L1160 220nH
C1164 NF
R1162 470
TR1155 BCW72
C1163 390p
C1165 NF
D1153 BBY31
CV1109 2-9p
L1158
C1174
R1164 4k7
R1163 10k
R1165 100k
+30V
R1129 39k
PV1102 100k
R1127 100k
R1126 100k
R1124 10k
R1130 82k
IC1101 LM258
C1150 1n
SPARE MATC
TUNING DIODES D1102-D1125, D1127, D1128, D1130 ARE MATCHED
D1102 BB405B
D1104 BB405B
D1106 BB405B
D1108 BB405B
C1104
C1106
C1105
C1102
R1101 1M
R1104 1M
C1111
CV1102 2-9p
C1107
C1109
D1103 BB405B
D1105 BB405B
C1108
D1107 BB405B
D1109 BB405B
R1102 1M
R1103 1M
C1110 390p
L1102
C1113 390p
R1105 3k9
TR1101 NE41137
R1108 47
R1109
C1115 390p
C1112 390p
R1106 1k
R1110
C1114 390p
L1103
CV1103 2-9p
D1110 BB405B
D1112 BB405B
C1119
C1121
C1120
C1117
R1111 1M
C1122
C1124
D1111 BB405B
D1113 BB405B
C1123
C1116
C1118 390p
R1112 1M
D1114 BB405B
D1116 BB405B
R1114 1M
C1126
CV1104 2-9p
D1115 BB405B
D1117 BB405B
R1113 1M
C11 390p
C1127
C1129
C1128
L1104
C1130
C1132
C1131
D1118 BB405B
D1120 BB405B
R1116 1M
C1133
C1134
D1119 BB405B
D1121 BB405B
R1115 1M

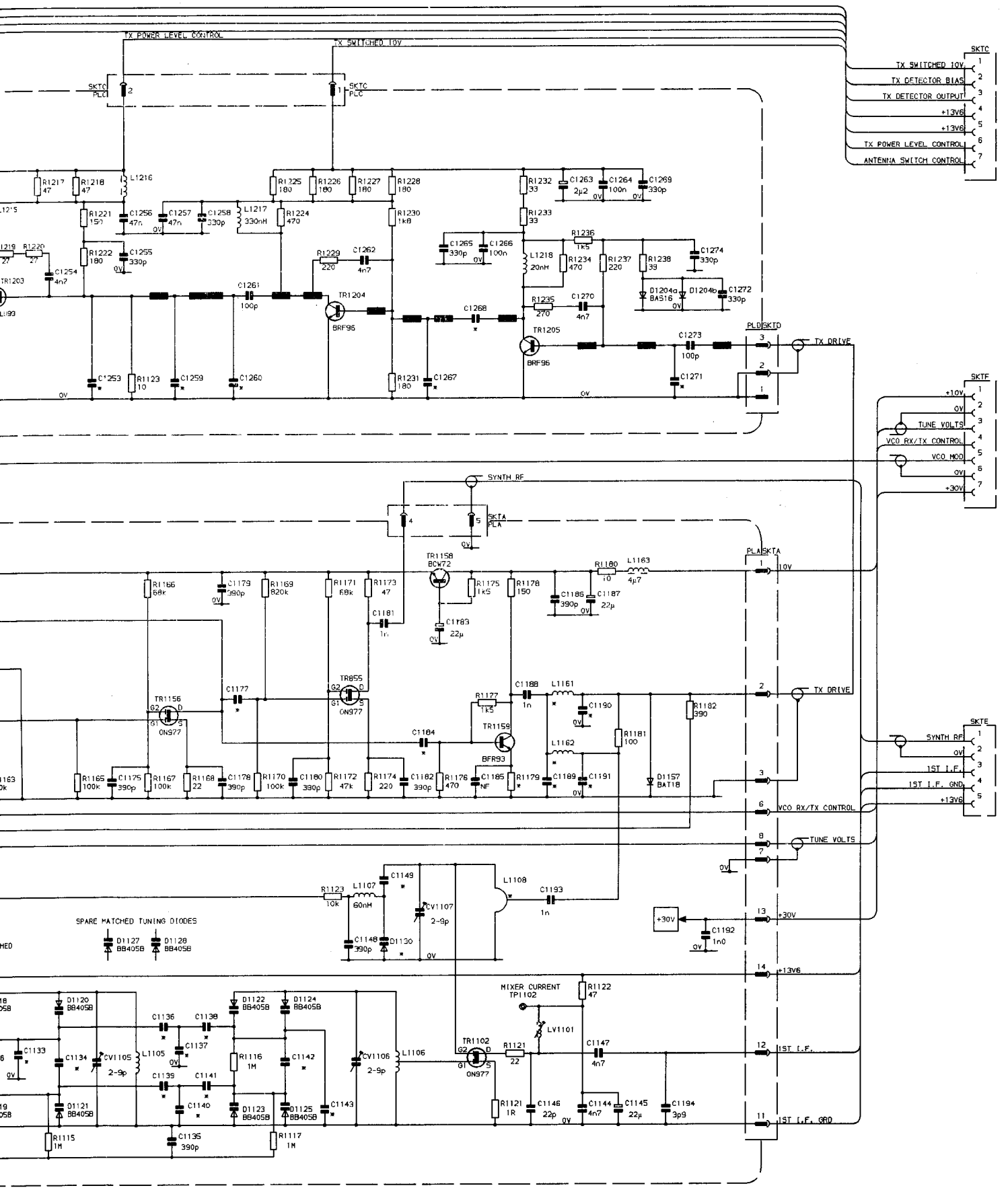
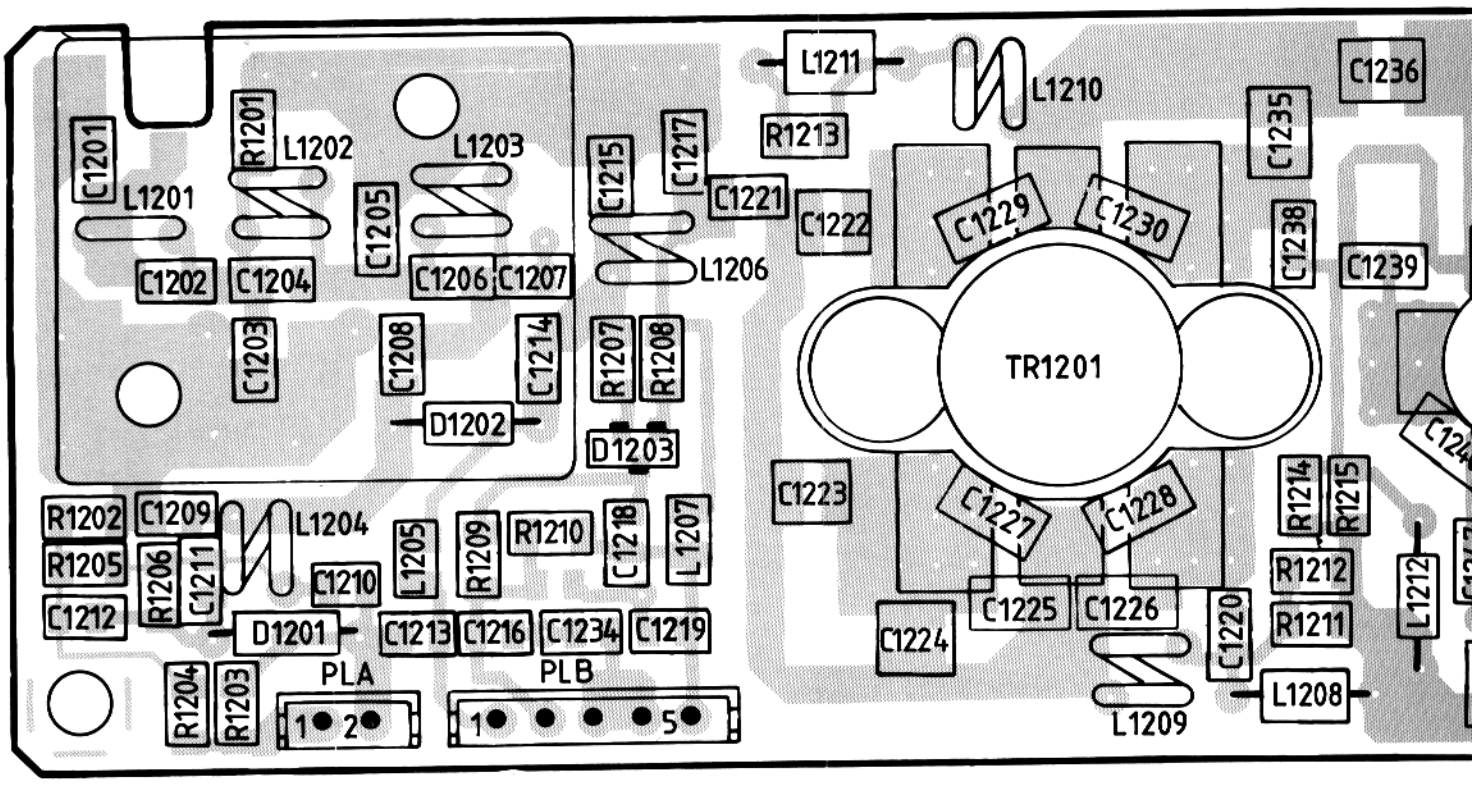
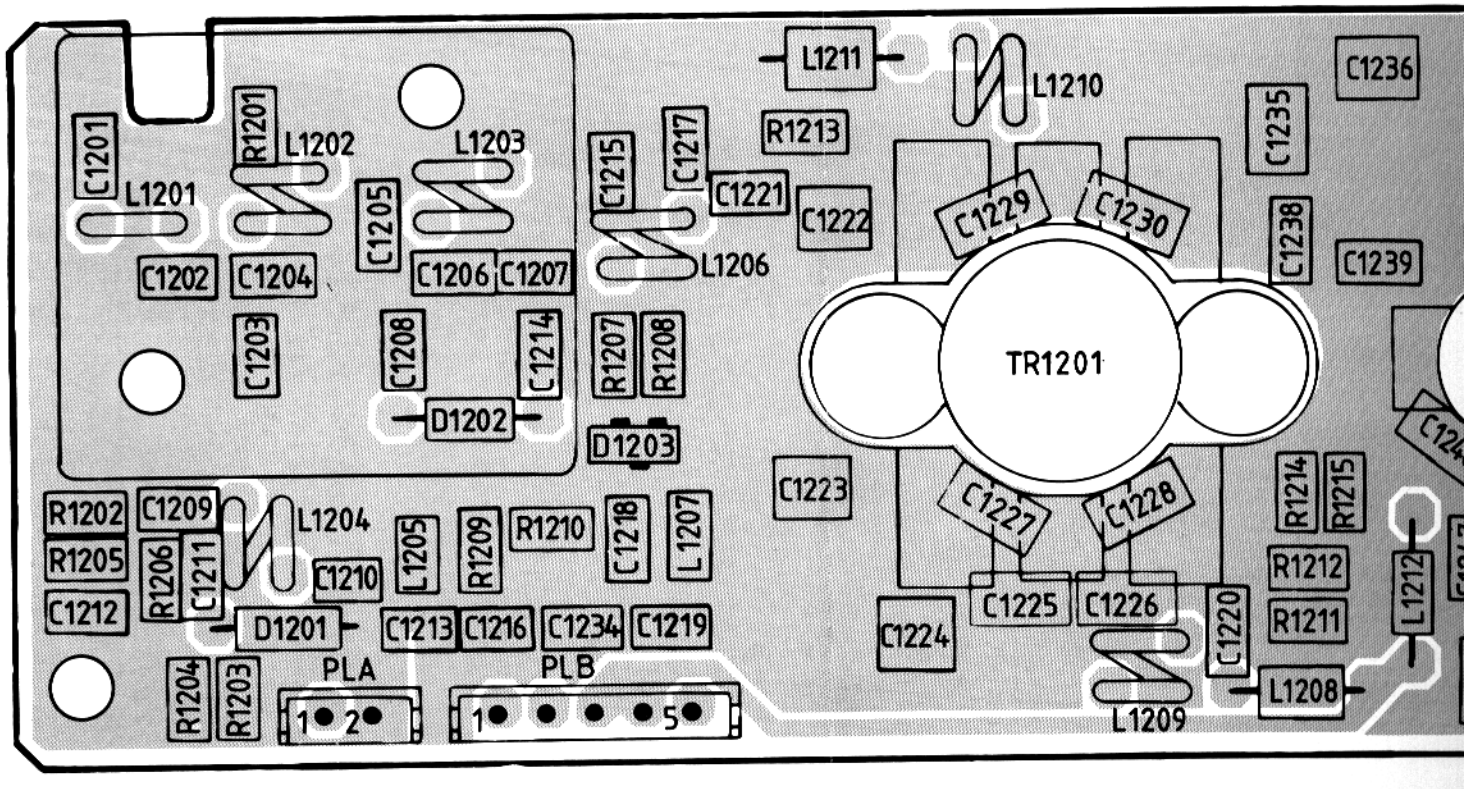
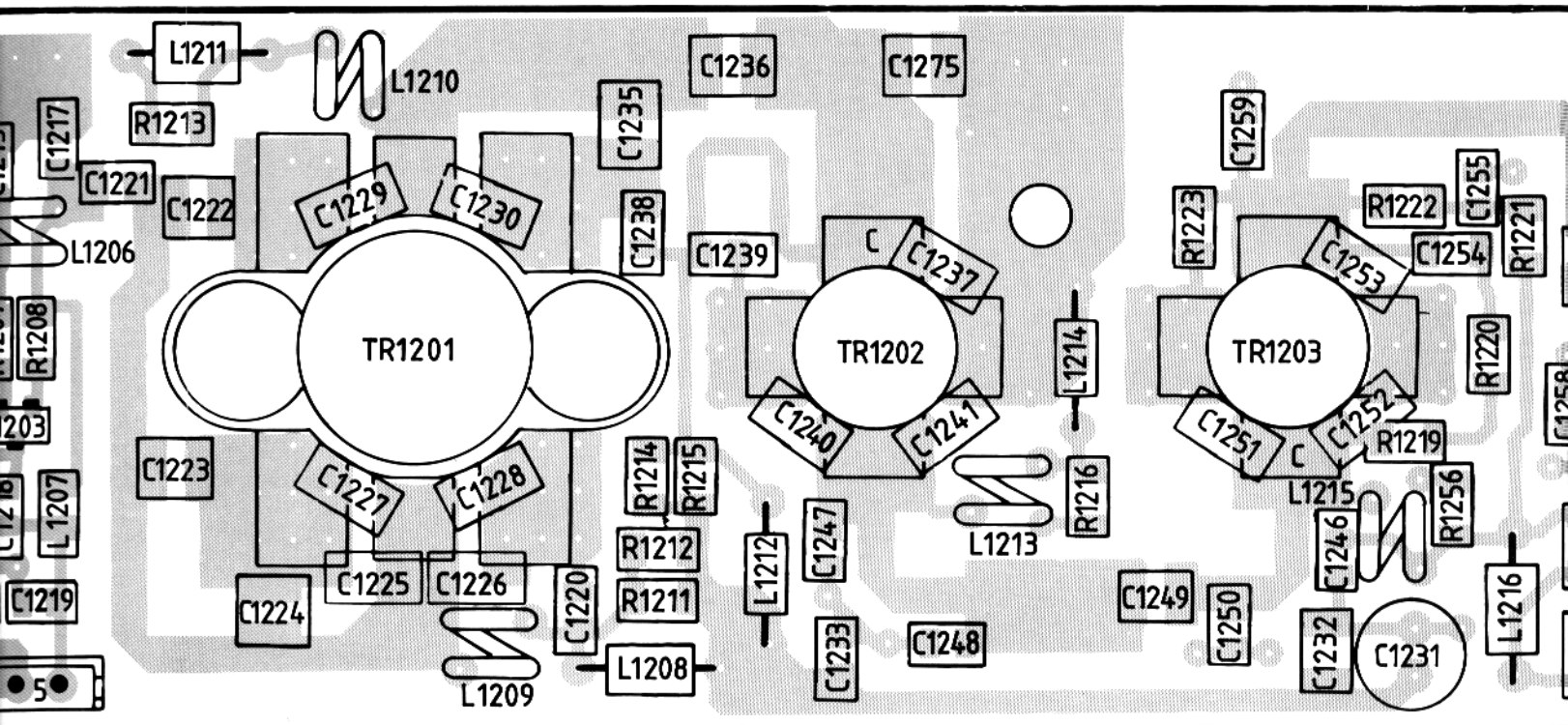


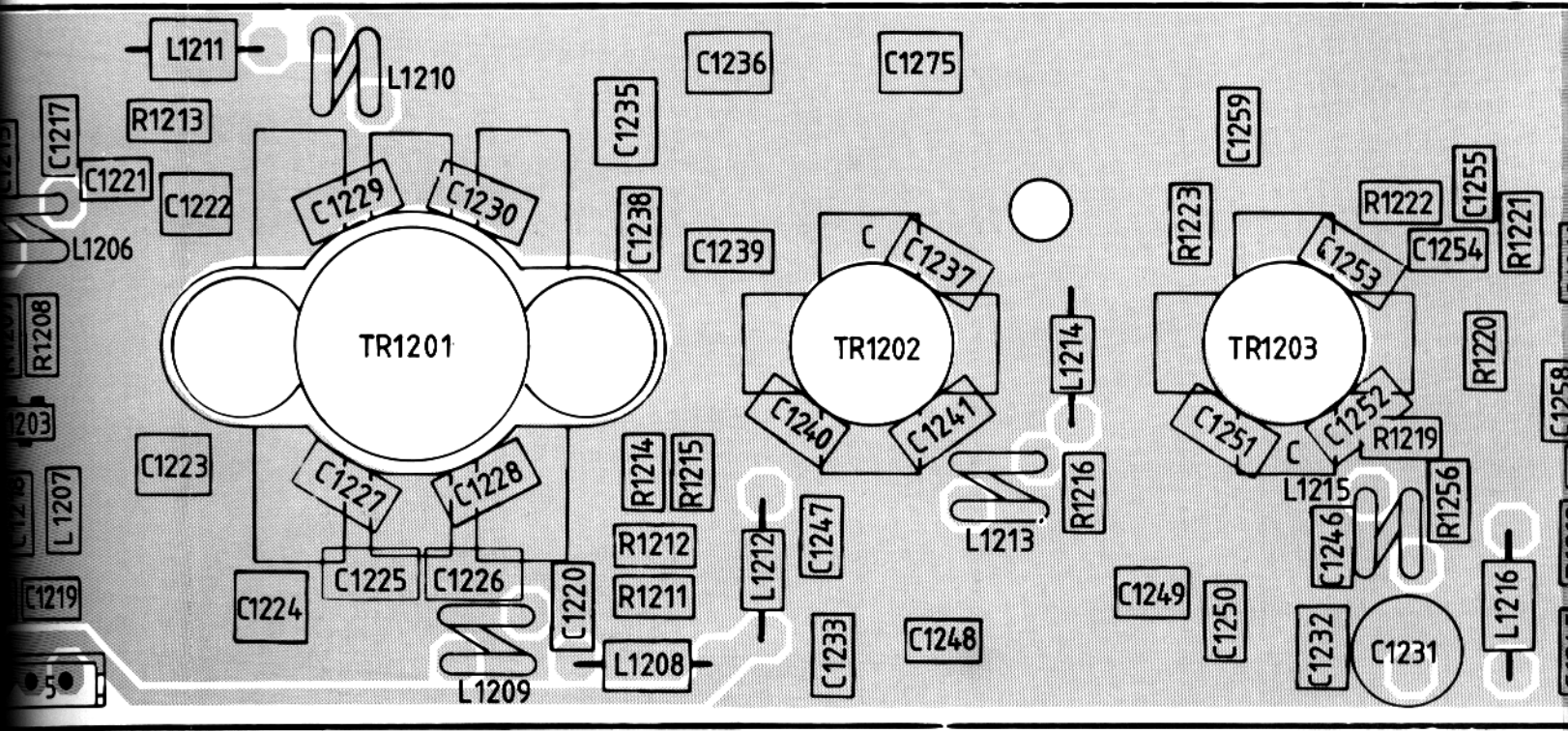
FIG 6.11A RF CIRCUIT DIAGRAM
(400-512MHz)

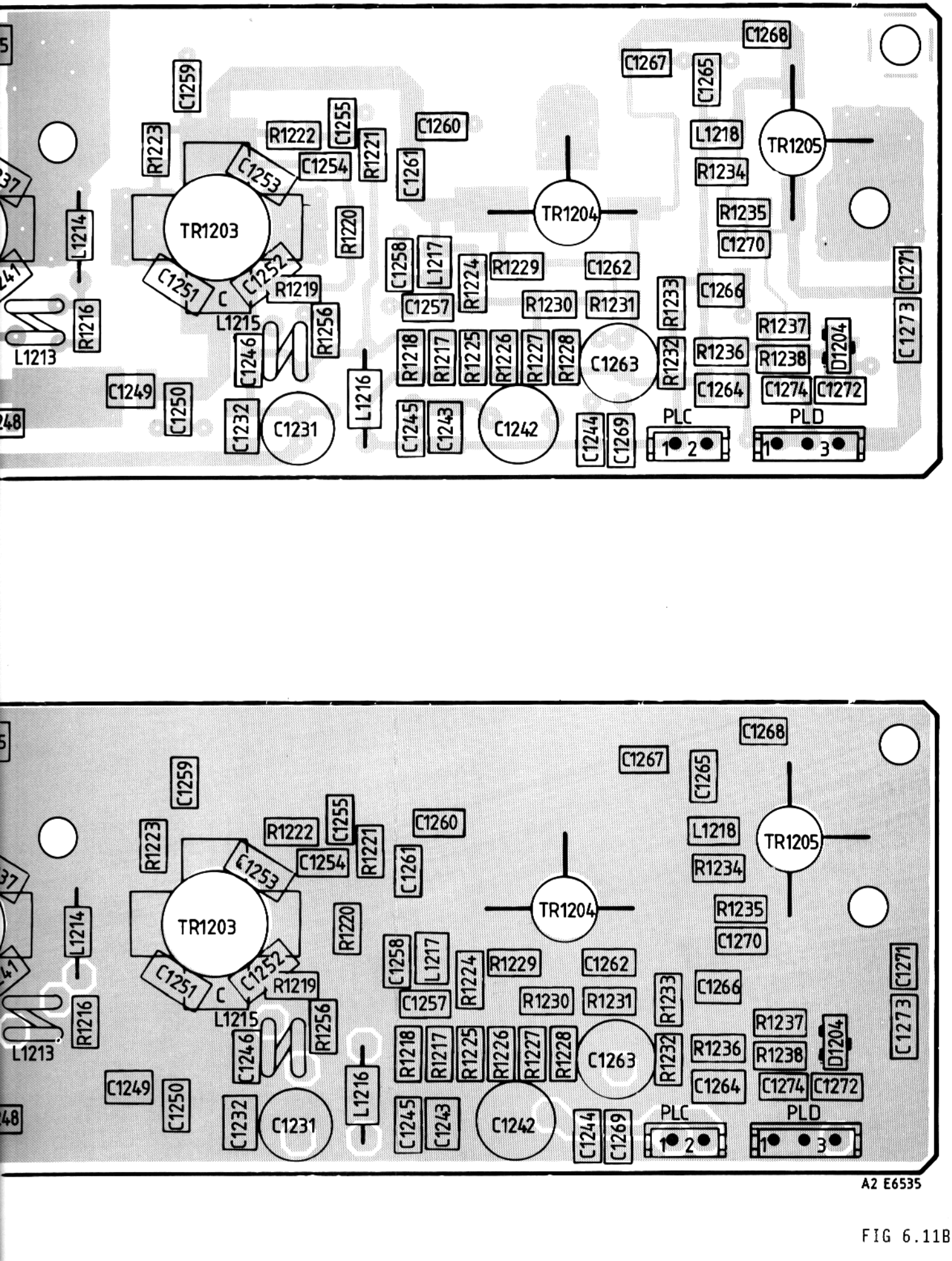
TP253/1


C1201
L1201
R1201
L1202
L1203
C1205
C1202
C1204
C1206
C1207
C1203
C1208
C1214
D1202
C1215
C1217
C1221
C1222
L1206
R1207
R1208
D1203
L1211
L1210
R1213
C1236
C1235
C1229
C1230
C1238
C1239
TR1201
C1223
C1227
C1228
R1214
R1215
R1202
C1209
L1204
R1205
R1206
C1211
C1210
C1205
R1209
R1210
C1218
L 1207
C1212
D1201
C1213
C1216
C1234
C1219
PLA
PLB
R1204
R1203
1 2
1 5
C1224
C1225
C1226
C1220
R1212
R1211
L1212
L1208
L1209


C1201
L1201
R1201
L1202
L1203
C1205
C1202
C1204
C1206
C1207
C1203
C1208
C1214
D1202
C1215
C1217
C1221
C1222
L1206
R1207
R1208
D1203
L1211
L1210
R1213
C1236
C1235
C1229
C1230
C1238
C1239
TR1201
C1223
C1227
C1228
R1214
R1215
R1202
C1209
L1204
R1205
R1206
C1211
C1210
C1205
R1209
R1210
C1218
L 1207
C1212
D1201
C1213
C1216
C1234
C1219
PLA
PLB
R1204
R1203
1 2
1 5
C1224
C1225
C1226
C1220
R1212
R1211
L1212
L1208
L1209

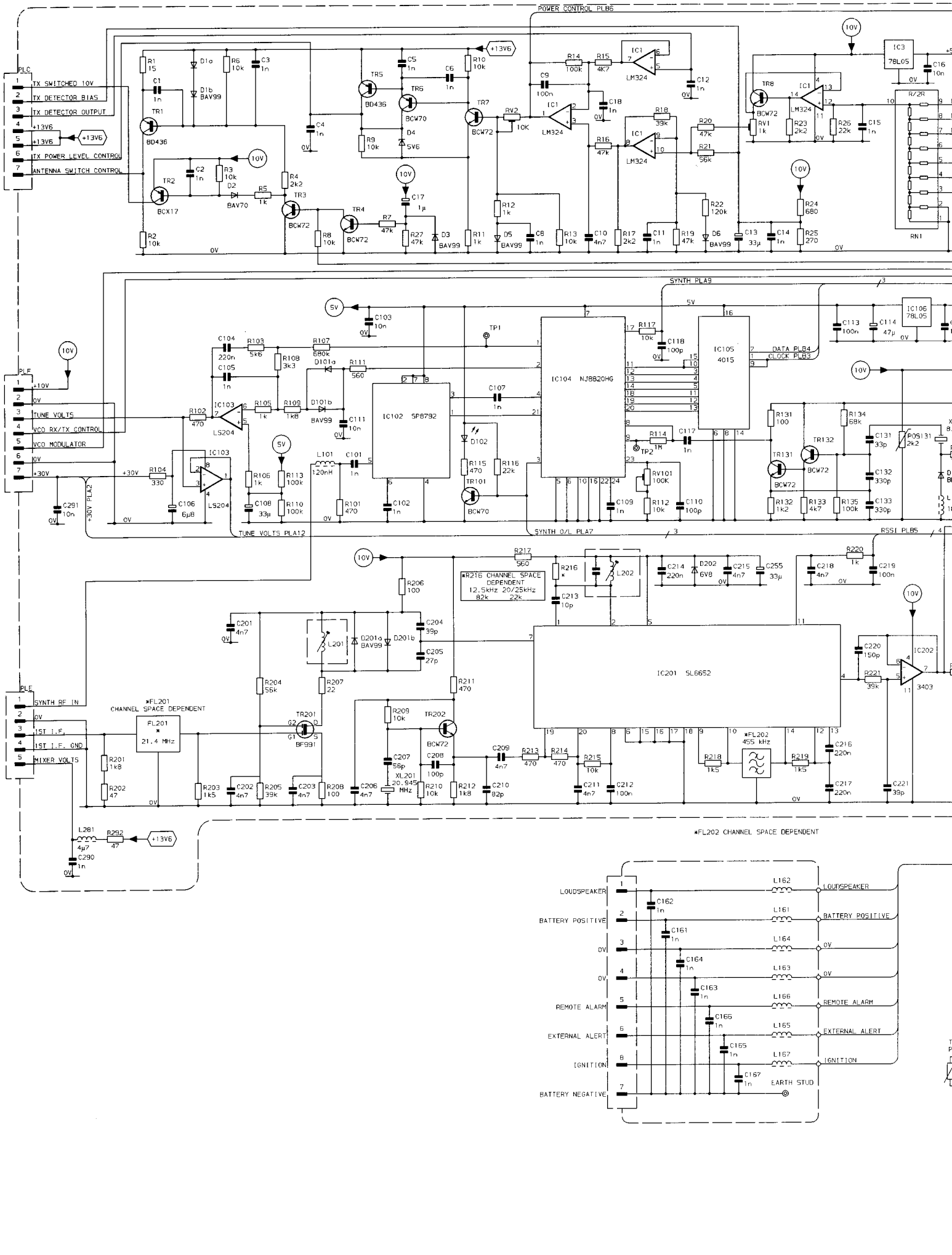

L1211
L1210
R1213
C1217
C1221
C1222
L1206
R1208
C1223
L1207
C1219
C1224
C1225
C1226
C1227
C1228
C1229
C1230
TR1201
C1235
C1238
C1236
C1275
C1239
C1237
TR1202
C1240
C1241
L1214
L1213
R1216
C1247
L1212
C1233
C1248
C1220
L1208
L1209
R1214
R1215
R1212
R1211
C1259
R1223
C1253
TR1203
C1251
C1252
C1254
C1255
R1222
R1221
R1220
R1219
L1215
R1256
C1246
C1249
C1250
C1232
C1231
L1216

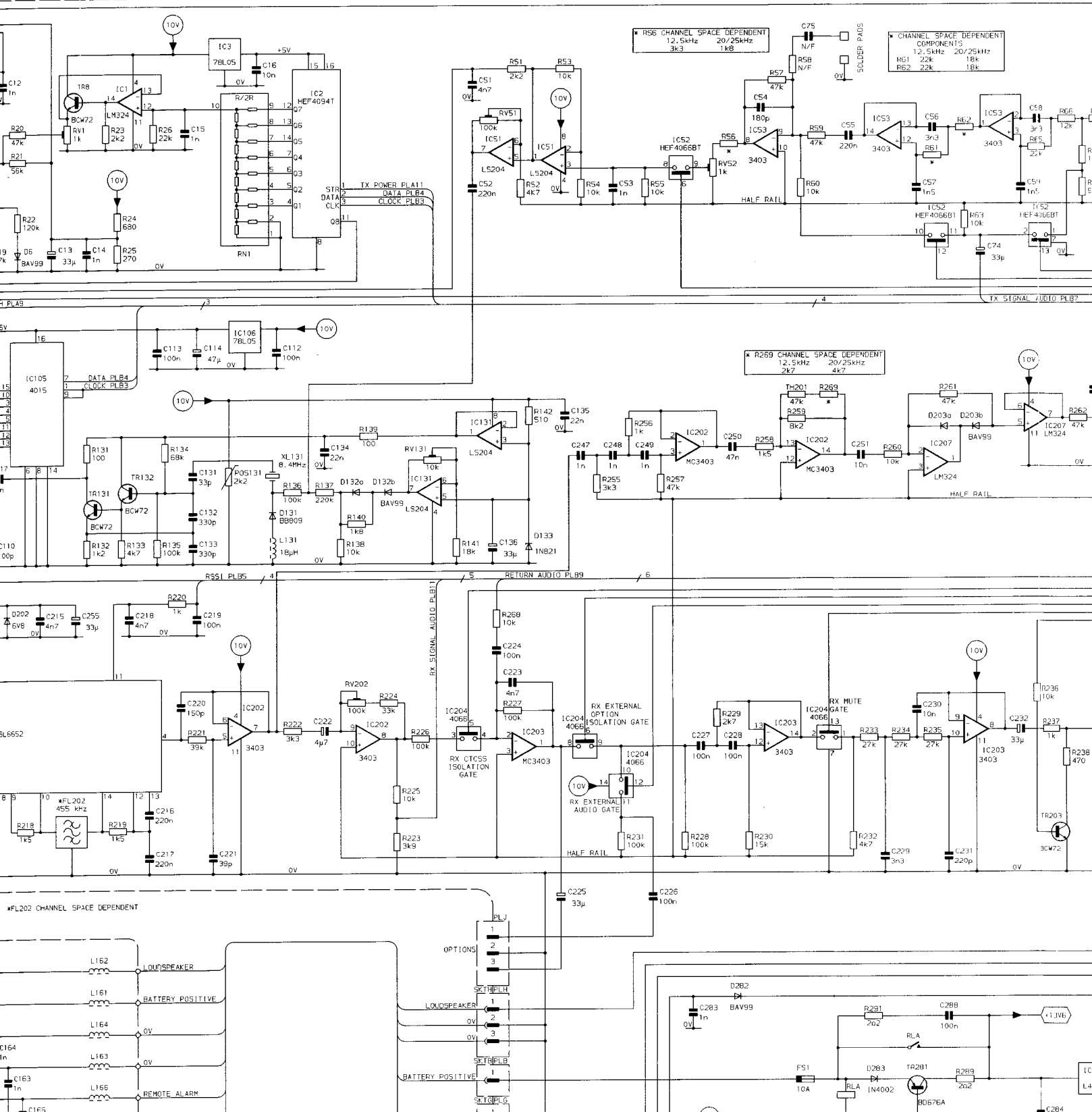

L1211
L1210
R1213
C1217
C1221
C1222
L1206
R1208
C1223
L1207
C1219
C1224
C1225
C1226
C1227
C1228
C1229
C1230
TR1201
C1235
C1238
C1236
C1275
C1239
C1237
TR1202
C1240
C1241
L1214
L1213
R1216
C1247
L1212
C1233
C1248
C1220
L1208
L1209
R1214
R1215
R1212
R1211
C1259
R1223
C1253
TR1203
C1251
C1252
C1254
C1255
R1222
R1221
R1220
R1219
L1215
R1256
C1246
C1249
C1250
C1232
C1231
L1216



A2 E6535

FIG 6.11B TRANSM
LOCATI


POWER CONTROL PLB6
PLC
1 TX SWITCHED 10V
2 TX DETECTOR BIAS
3 TX DETECTOR OUTPUT
4 +13V6
5 +13V6
6 TX POWER LEVEL CONTROL
7 ANTENNA SWITCH CONTROL
SYNTH PLA9
PLE
1 +10V
2 0V
3 TUNE VOLTS
4 VCO RX/TX CONTROL
5 VCO MODULATOR
6 0V
7 +30V
TUNE VOLTS PLA12
SYNTH O/L PLA7
RSSI PLB5
DATA PLB4
CLOCK PLB3
IC104 NJ88820HG
IC102 SP8792
IC105 4015
IC201 SL6652
IC103 LS204
IC106 78L05
IC3 78L05
LM324
BD436
BCW70
BCW72
BCX17
BAV70
BAV99
BF991
3403
R/2R
RN1
*R216 CHANNEL SPACE DEPENDENT
12.5kHz 20/25kHz
82k 22k
*FL201
CHANNEL SPACE DEPENDENT
FL201
*
21.4 MHz
*FL202
455 kHz
XL201
20.945
MHz
*FL202 CHANNEL SPACE DEPENDENT
LOUDSPEAKER
BATTERY POSITIVE
0V
0V
REMOTE ALARM
EXTERNAL ALERT
IGNITION
BATTERY NEGATIVE
EARTH STUD


* R56 CHANNEL SPACE DEPENDENT
12.5kHz 20/25kHz
3k3 1k8
* CHANNEL SPACE DEPENDENT COMPONENTS
12.5kHz 20/25kHz
RG1 22k 18k
RG2 22k 18k
* R269 CHANNEL SPACE DEPENDENT
12.5kHz 20/25kHz
2k7 4k7
*FL202 CHANNEL SPACE DEPENDENT
TX SIGNAL AUDIO PLB7
RSSI PLB5
RETURN AUDIO PLB9
RX SIGNAL AUDIO PLB11
HALF RAIL
RX EXTERNAL OPTION ISOLATION GATE
RX MUTE GATE
RX CTCSS ISOLATION GATE
RX EXTERNAL AUDIO GATE
TX POWER PLA11
DATA PLB4
CLOCK PLB3
LOUDSPEAKER
BATTERY POSITIVE
REMOTE ALARM
EXTERNAL ALERT
IGNITION
EARTH STUD
TH1 FITTED TO P.A. HEATSINK
SOLDER PADS
IC1 LM324
IC2 HEF4094T
IC3 78L05
IC51 LS204
IC52 HEF4066BT
IC53 3403
IC105 4015
IC106 78L05
IC131 LS204
IC202 MC3403
IC203 MC3403
IC204 4066
IC207 LM324
TR8 BCW72
TR131 BCW72
TR132 BCW72
TR203 BC672
TR281 BD676A
D131 BB809
D132a D132b BAV99
D202 6V8
D203a D203b BAV99
D281a BAV70
D281b
D282 BAV99
D283 IN4002
D133 1N821
L131 18µH
L161
L162
L163
L164
L165
L166
L167
XL131 8.4MHz
POS131 2k2
RV1 1k
RV51 100k
RV52 1k
RV131 10k
RV202 100k
RN1 R/2R
FS1 10A
RLA
PL1
SKT8PLH
SKT8PLB
SKT8PLG
OPTIONS
0V
10V
+5V
+13V6

FIG

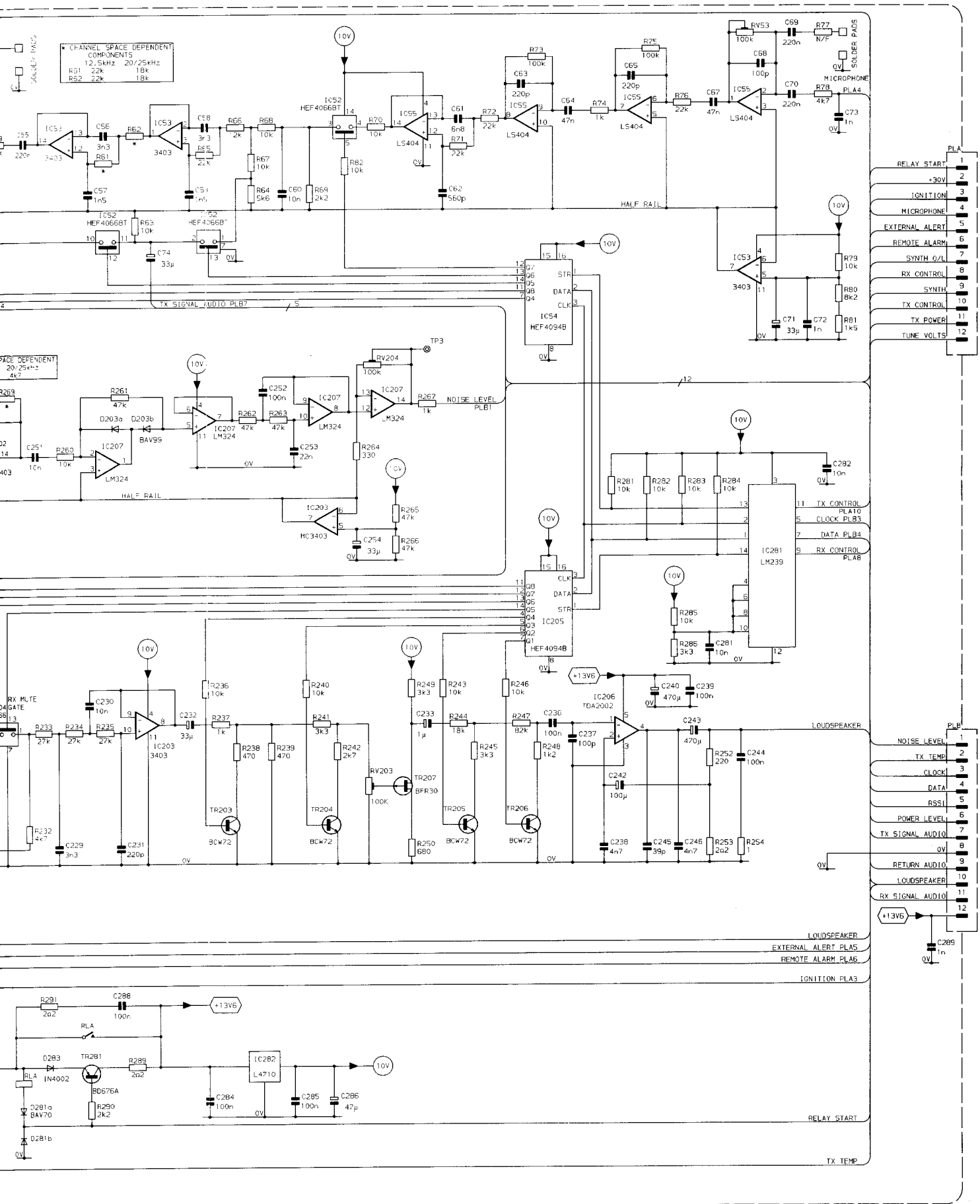
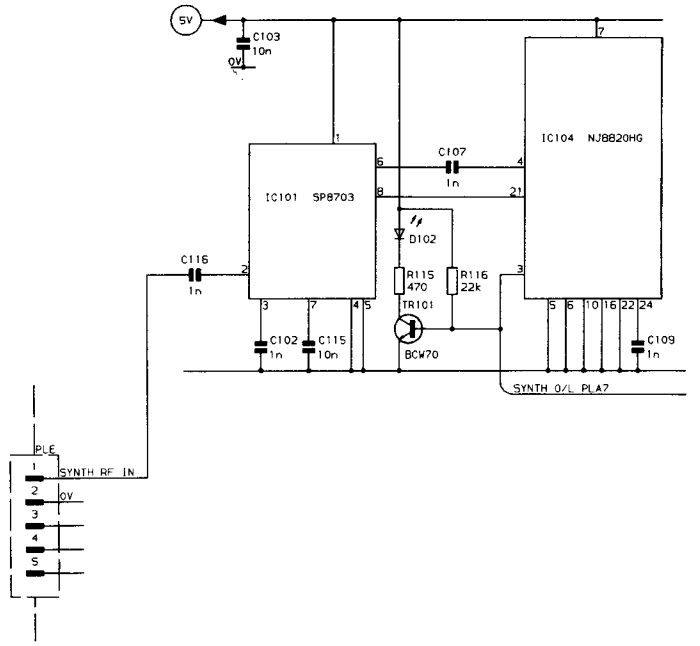
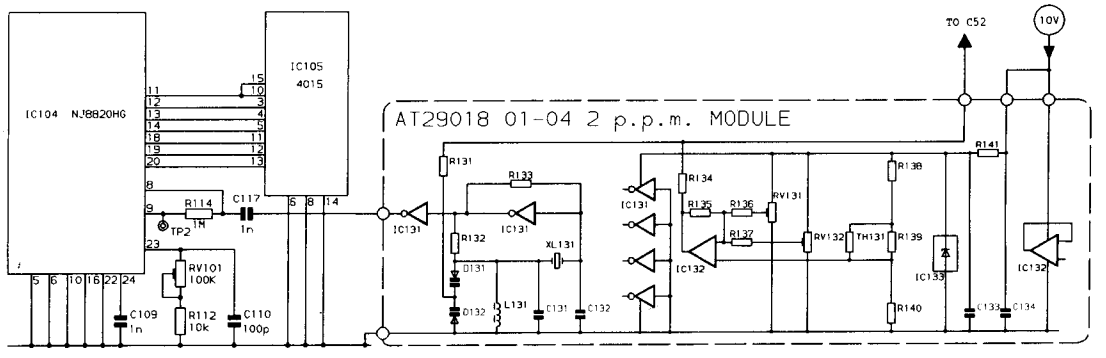


FIG 6.12 ANALOGUE PWB CIRCUIT DIAGRAM

TP253

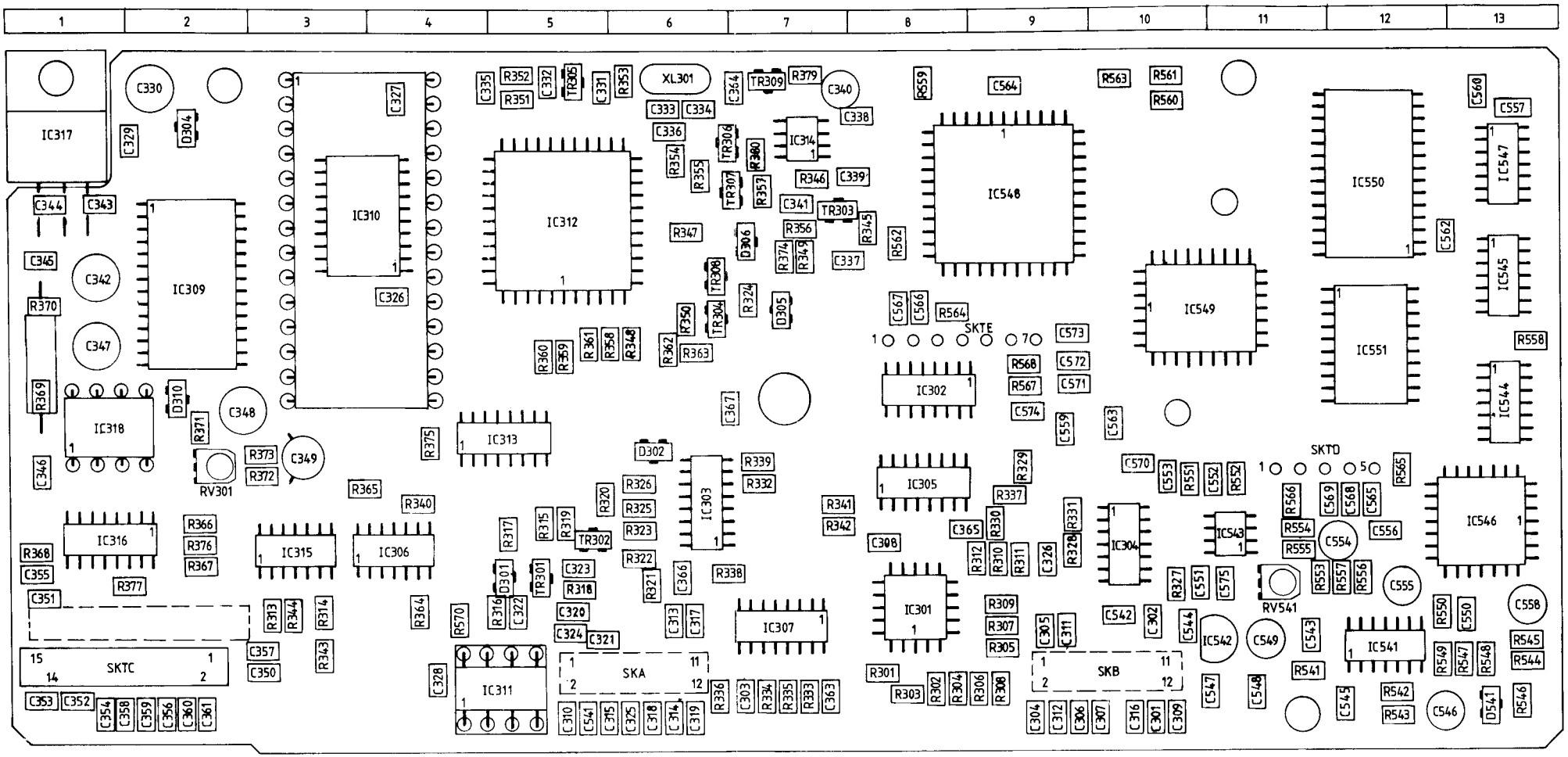


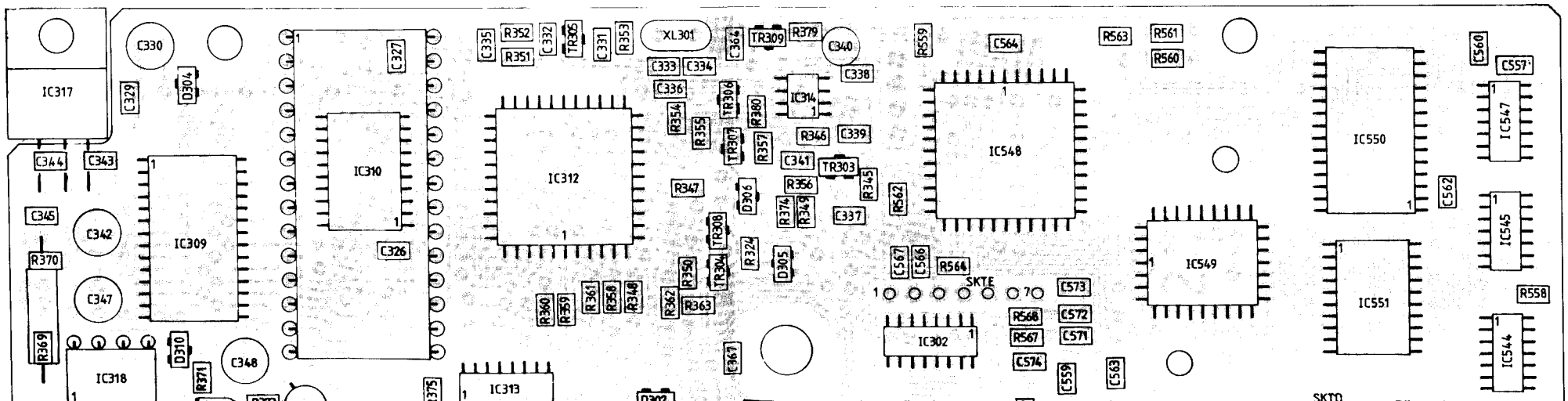
UHF PRESCALER (IC101)

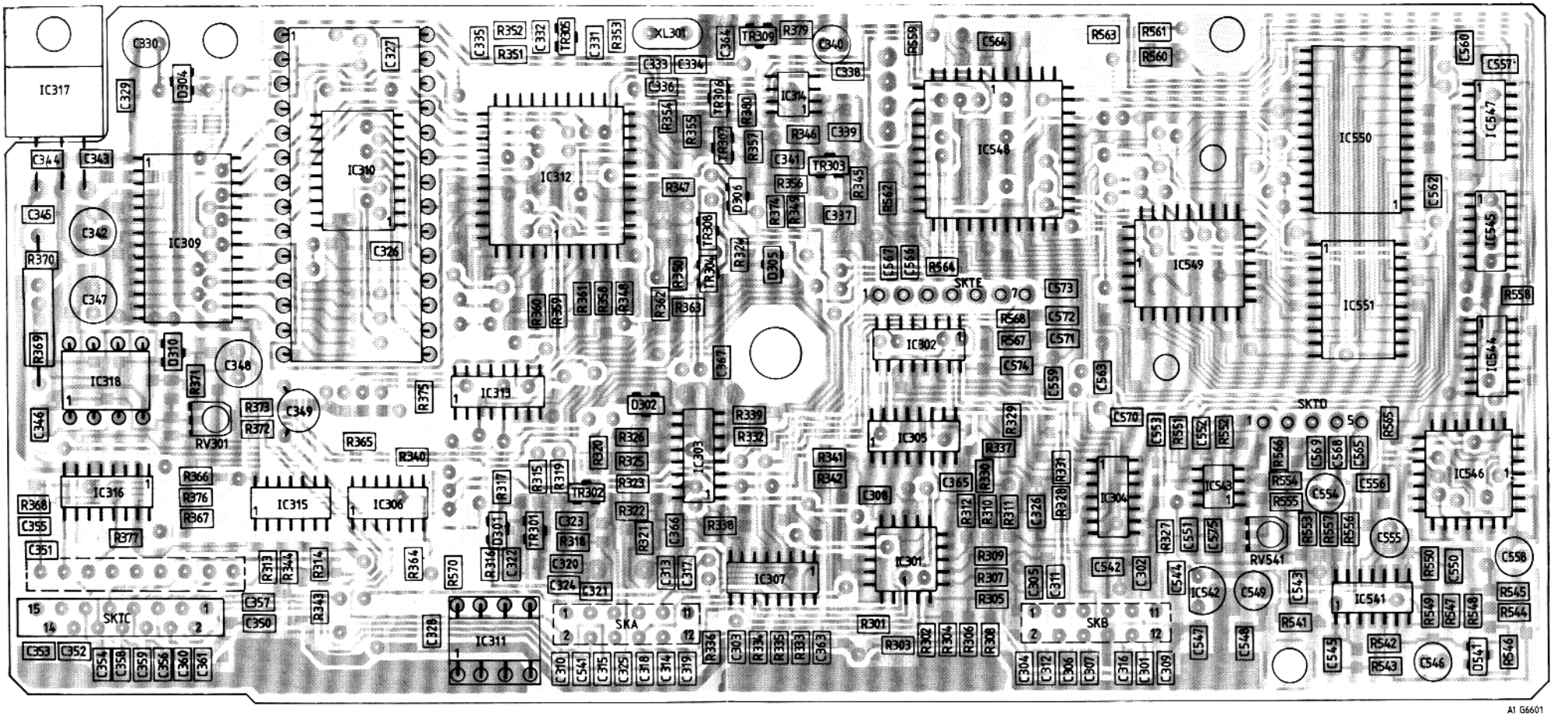


±2ppm REFERENCE OSCILLATOR MODULE

FIG 6.13 ANALOGUE PWB CIRCUIT VARIATIONS

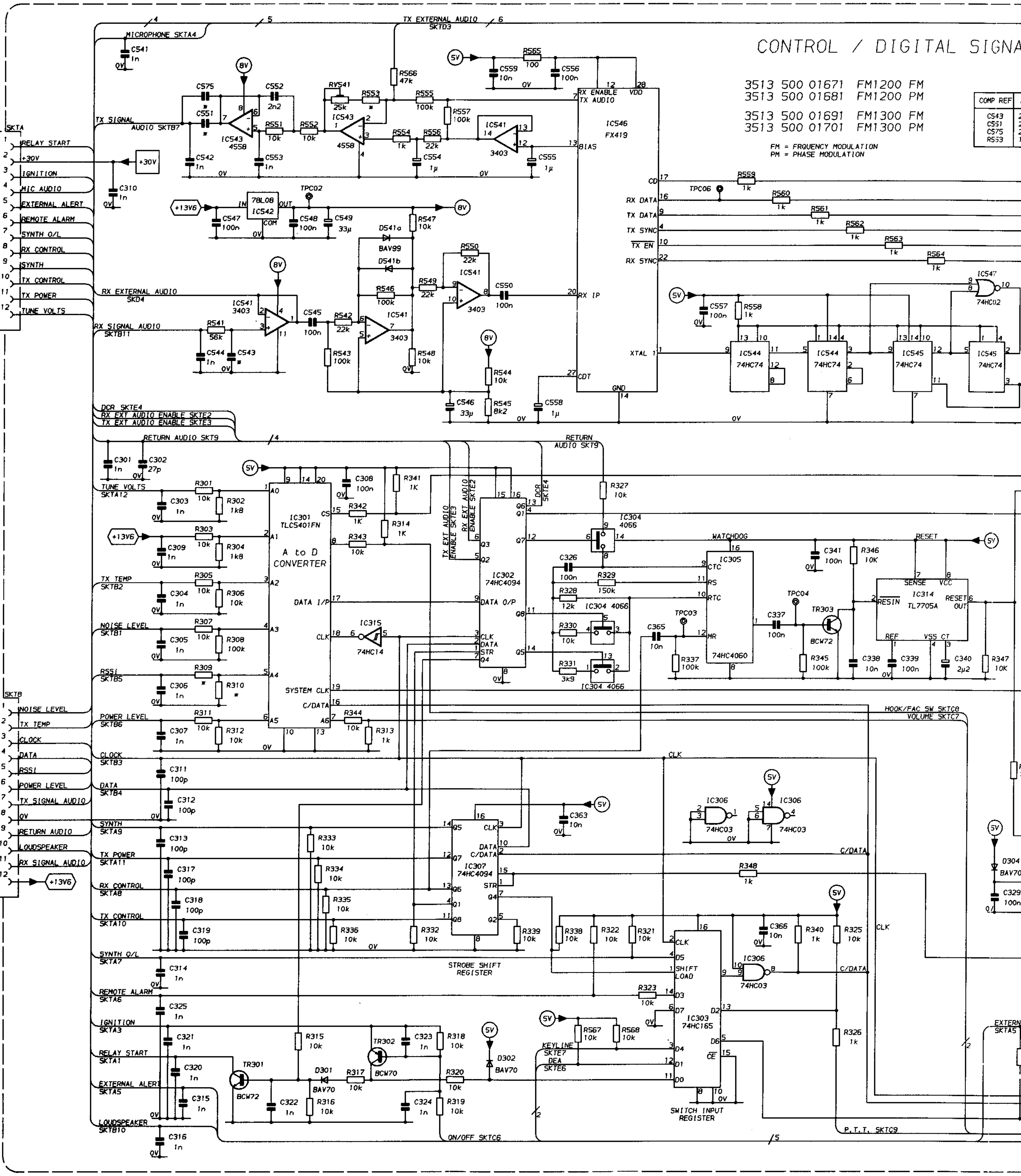

1 2 3 4 5 6 7 8 9 10 11 12 13
A B C D E F
IC317
IC310
IC309
IC312
XL301
IC314
IC548
IC550
IC547
IC545
IC549
IC551
IC544
IC318
IC313
IC302
IC303
IC305
IC304
IC543
IC546
IC316
IC315
IC306
IC307
IC301
IC542
IC541
IC311
RV301
RV541
SKTC
SKA
SKB
SKTE
SKTD


IC317
IC310
IC309
IC312
XL301
IC314
IC548
IC550
IC547
IC545
IC549
IC551
IC544
IC318
IC313
IC302
SKTE
SKTD



A1 G6601

FIG 6.1 CONTROL/DIGITAL SIGNALLING PWB COMPONENT LOCATION DIAGRAM


CONTROL / DIGITAL SIGNA
3513 500 01671 FM1200 FM
3513 500 01681 FM1200 PM
3513 500 01691 FM1300 FM
3513 500 01701 FM1300 PM
FM = FREQUENCY MODULATION
PM = PHASE MODULATION
COMP REF
C543
C551
C575
R553
SKTA
RELAY START
+30V
IGNITION
MIC AUDIO
EXTERNAL ALERT
REMOTE ALARM
SYNTH O/L
RX CONTROL
SYNTH
TX CONTROL
TX POWER
TUNE VOLTS
SKTB
NOISE LEVEL
TX TEMP
CLOCK
DATA
RSSI
POWER LEVEL
TX SIGNAL AUDIO
0V
RETURN AUDIO
LOUDSPEAKER
RX SIGNAL AUDIO
+13V6
MICROPHONE SKTA4
TX EXTERNAL AUDIO SKTD3
TX SIGNAL AUDIO SKTB7
RX EXTERNAL AUDIO SKD4
RX SIGNAL AUDIO SKTB11
IC546 FX419
RX ENABLE
TX AUDIO
VDD
BIAS
RX IP
XTAL
CDT
GND
RX DATA
TX DATA
TX SYNC
TX EN
RX SYNC
IC542 78L08
IC543 4558
IC541 3403
IC544 74HC74
IC545 74HC74
IC547 74HC02
DCR SKTE4
RX EXT AUDIO ENABLE SKTE2
TX EXT AUDIO ENABLE SKTE3
RETURN AUDIO SKT9
IC301 TLC5401FN
A to D CONVERTER
DATA I/P
SYSTEM CLK
C/DATA
IC302 74HC94094
IC304 4066
IC305 74HC4060
WATCHDOG
RESET
IC314 TL7705A
SENSE
VCC
RESIN
RESET OUT
REF
VSS CT
TR303 BCW72
IC315 74HC14
HOOK/FAC SW SKTC8
VOLUME SKTC7
CLK
IC306 74HC03
IC307 74HC4094
STROBE SHIFT REGISTER
IC303 74HC165
SHIFT LOAD
SWITCH INPUT REGISTER
KEYLINE SKTE7
DEA SKTE6
TR301 BCW72
TR302 BCW70
D301 BAV70
D302 BAV70
D304 BAV70
ON/OFF SKTC6
P.T.T. SKTC9
EXTERNAL SKTA5

CONTROL / DIGITAL SIGNALLING ASSEMBLY

3513 500 01671 FM1200 FM
3513 500 01681 FM1200 PM

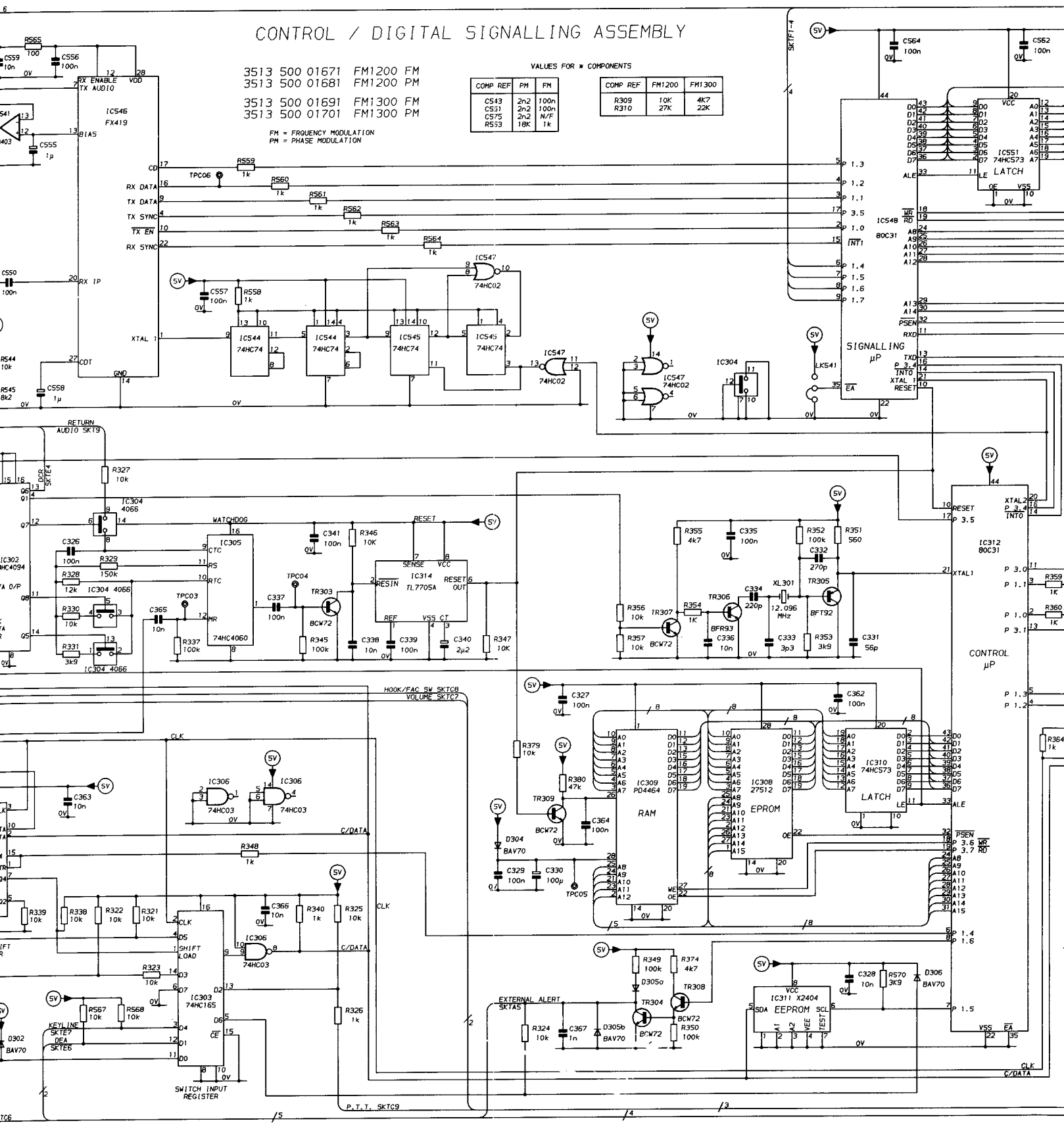
3513 500 01691 FM1300 FM
3513 500 01701 FM1300 PM

FM = FRQUENCY MODULATION
PM = PHASE MODULATION

VALUES FOR * COMPONENTS

COMP REF	PM	FM
C543	2n2	100n
C531	2n2	100n
C575	2n2	N/F
R533	18K	1k

COMP REF	FM1200	FM1300
R309	10K	4K7
R310	27K	22K



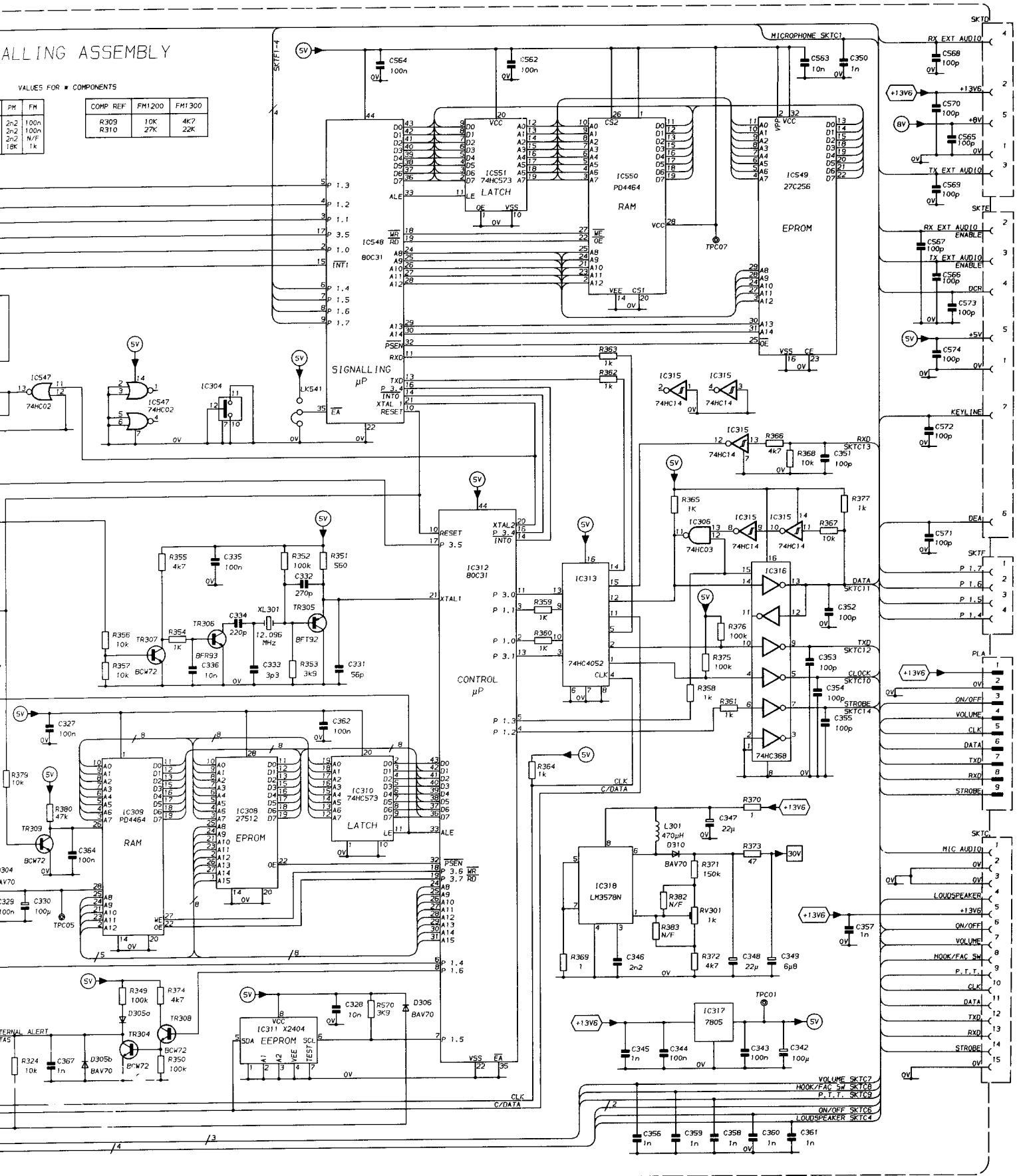
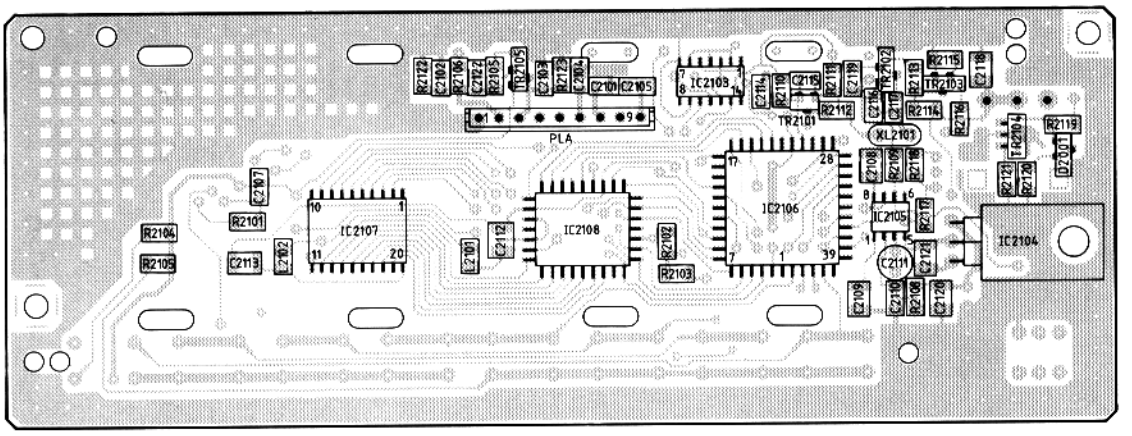
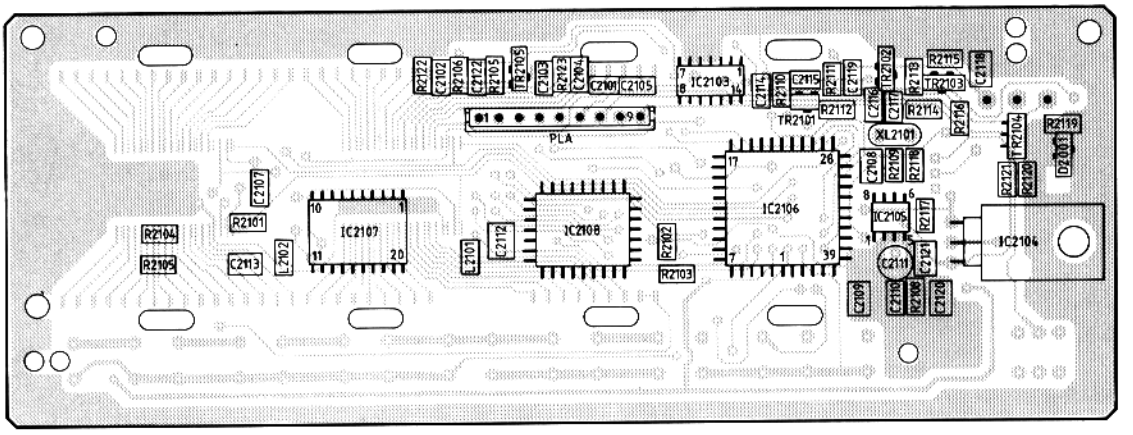
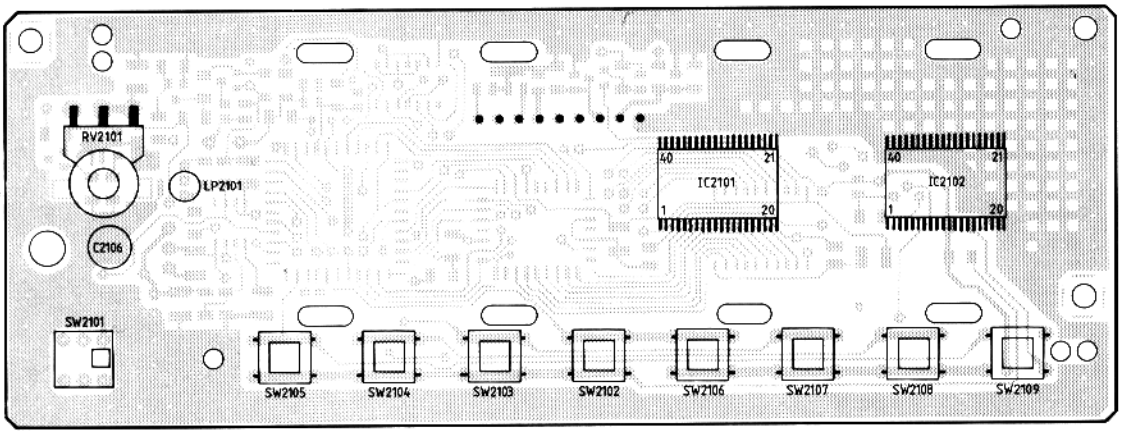


FIG 6.2 CONTROL/DIGITAL SIGNALLING PWB CIRCUIT DIAGRAM







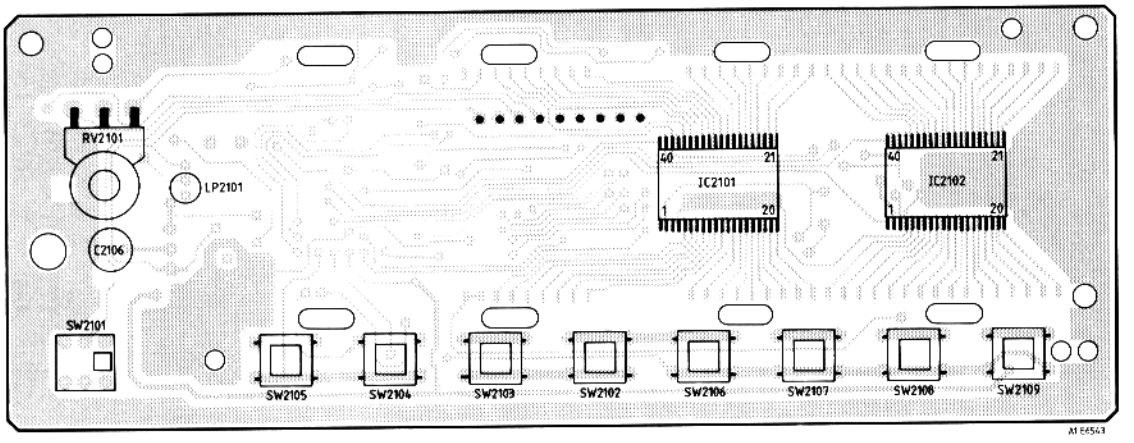
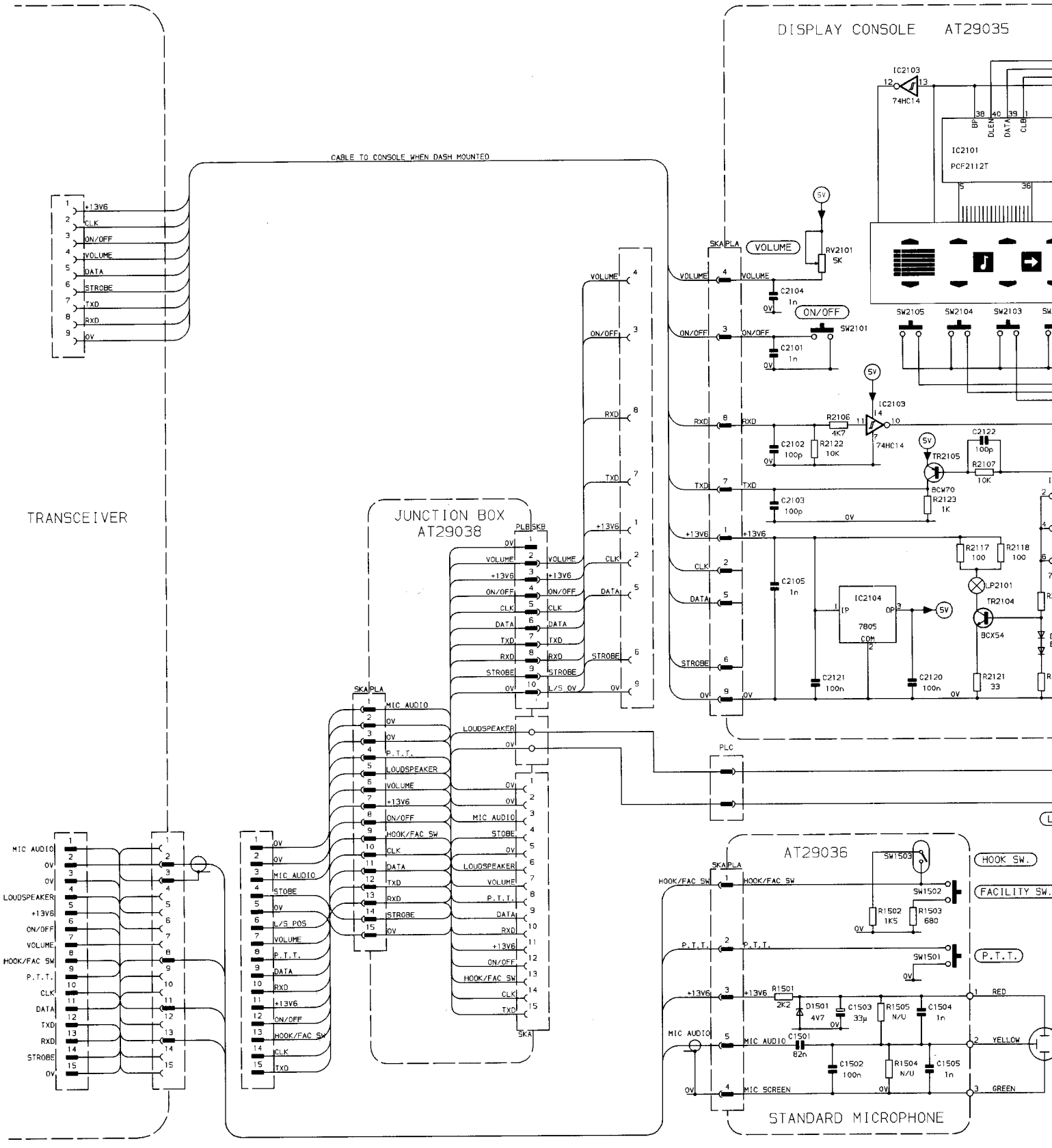
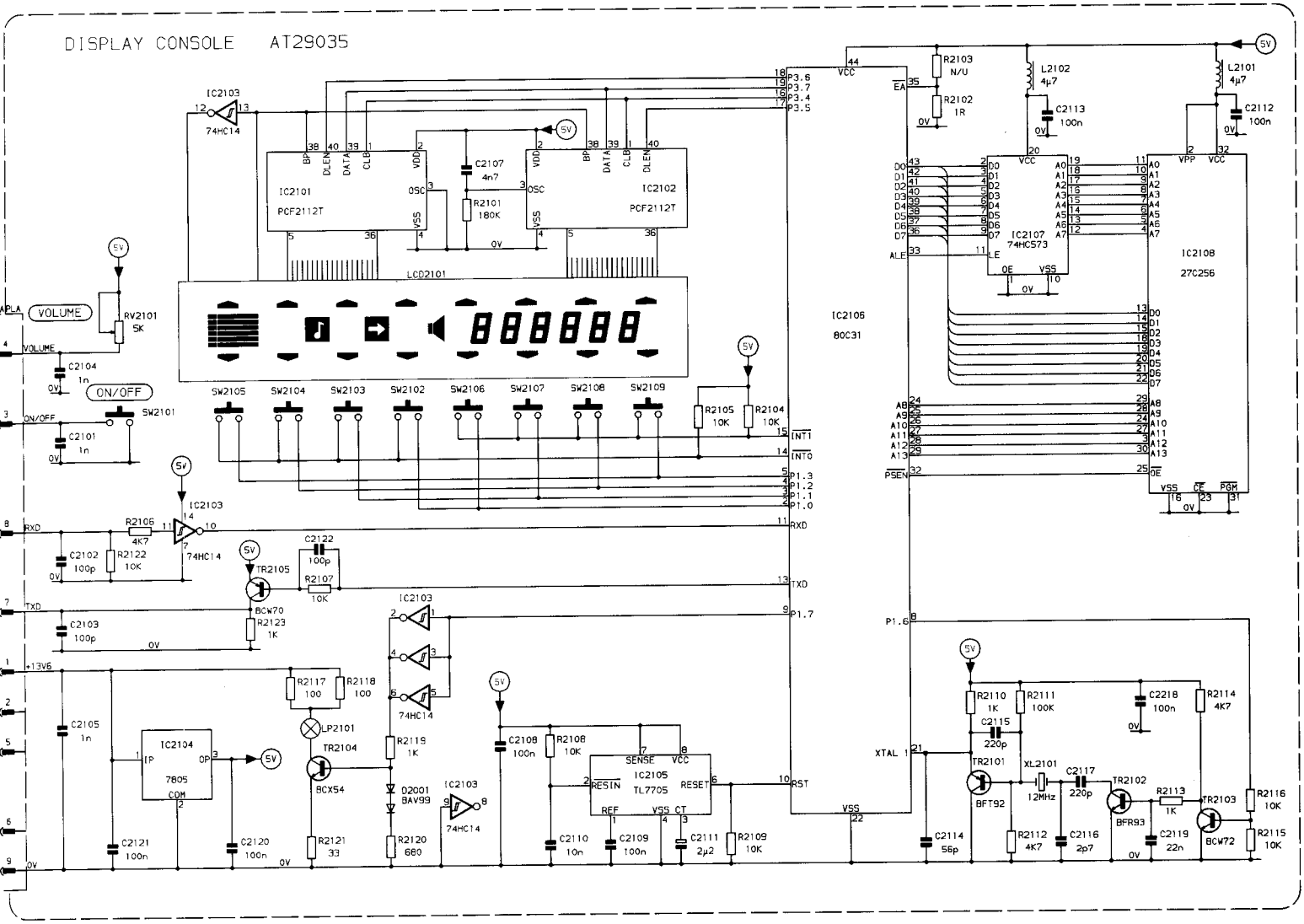


FIG 6.15 DISPLAY CONSOLE
COMPONENT LOCATION DIAGRAM


TRANSCEIVER
CABLE TO CONSOLE WHEN DASH MOUNTED
+13V6
CLK
ON/OFF
VOLUME
DATA
STROBE
TXD
RXD
0V
JUNCTION BOX
AT29038
PLB
SKB
SKA
PLA
MIC AUDIO
P.T.T.
LOUDSPEAKER
HOOK/FAC SW
L/S POS
L/S 0V
DISPLAY CONSOLE AT29035
IC2103
74HC14
IC2101
PCF2112T
RV2101
5K
SW2101
SW2105
SW2104
SW2103
R2106
4K7
R2122
10K
C2102
100p
C2103
100p
C2104
1n
C2101
1n
C2105
1n
TR2105
BCW70
R2123
1K
C2122
100p
R2107
10K
R2117
100
R2118
100
LP2101
TR2104
BCX54
IC2104
7805
R2121
33
C2120
100n
C2121
100n
PLC
AT29036
SW1503
SW1502
SW1501
R1502
1K5
R1503
680
R1501
2K2
D1501
4V7
C1503
33µ
R1505
N/U
C1504
1n
C1501
82n
C1502
100n
R1504
N/U
C1505
1n
HOOK SW.
FACILITY SW.
P.T.T.
STANDARD MICROPHONE
RED
YELLOW
GREEN
MIC SCREEN



NOTES

1. CONSOLE AND MICROPHONE SHOWN IN DASH MOUNT CONFIGURATION.
2. LOUDSPEAKER SHOWN IN REMOTE MOUNT CONFIGURATION.

FIG 6.16 DISPLAY CONSOLE & JUNCTION BOX CIRCUIT DIAGRAM

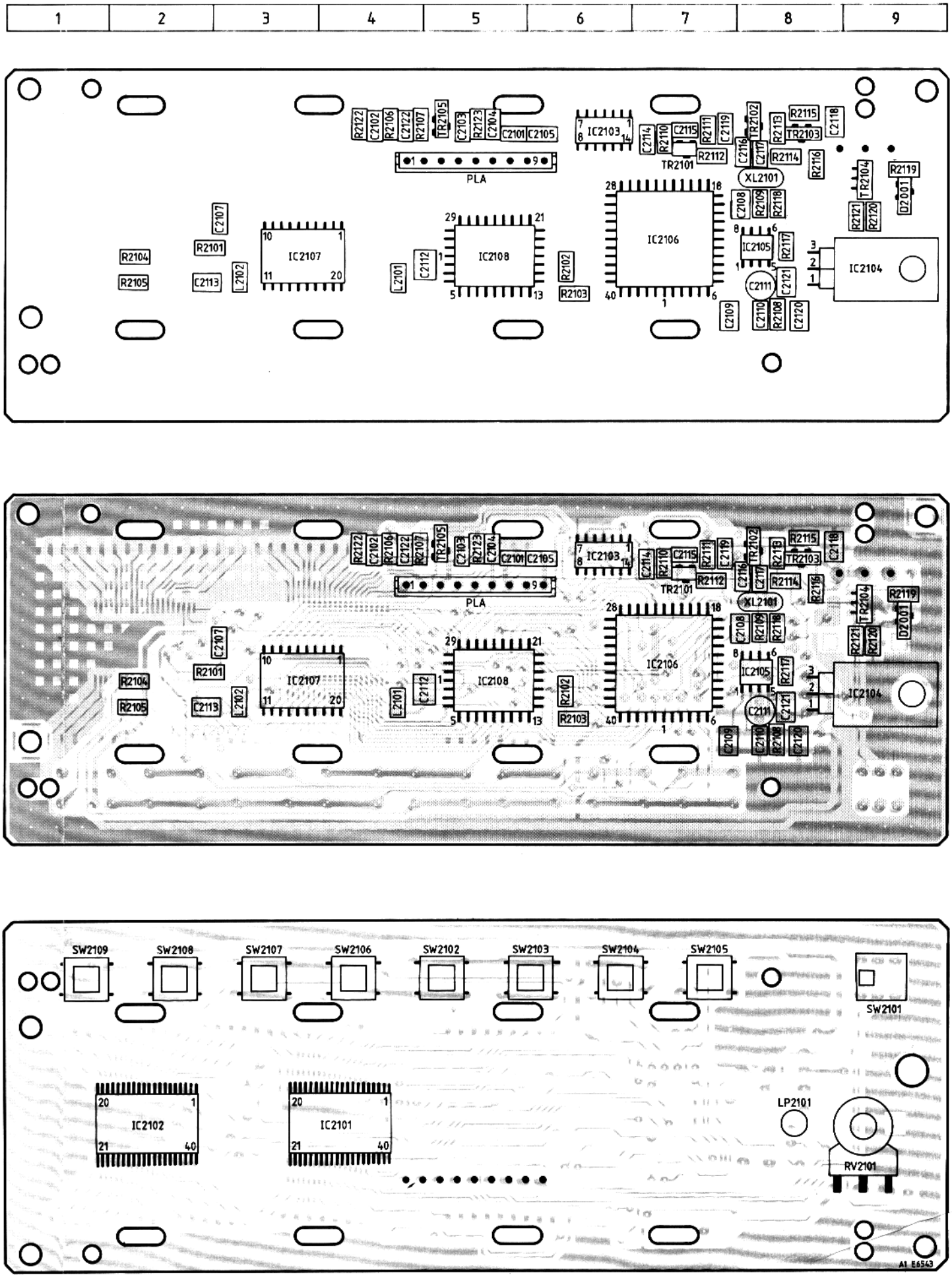
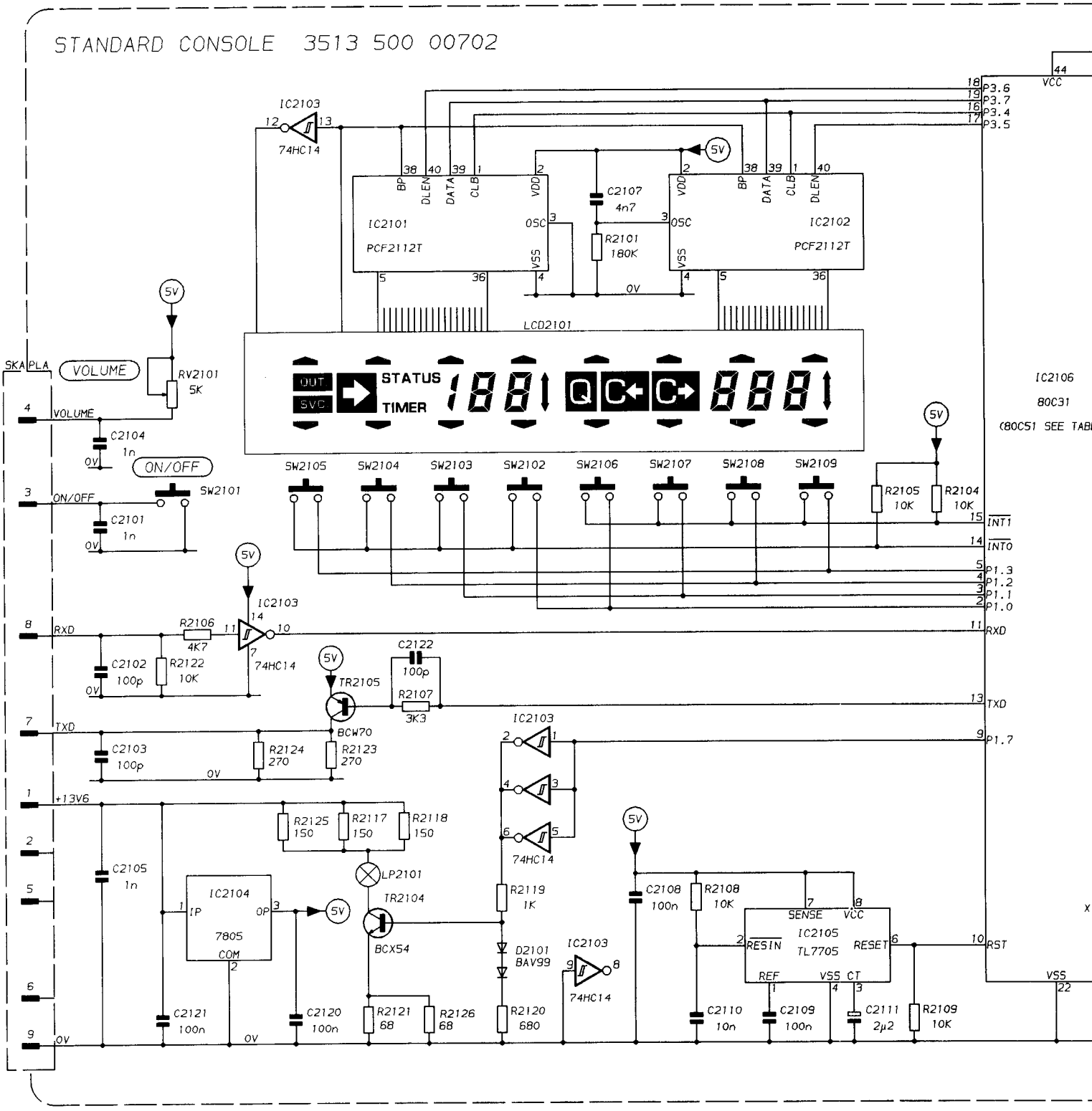


FIG 6.5 FM1200/FM1300 STANDARD CONSOLE COMPONENT LOCATION DIAGRAM

TP253A



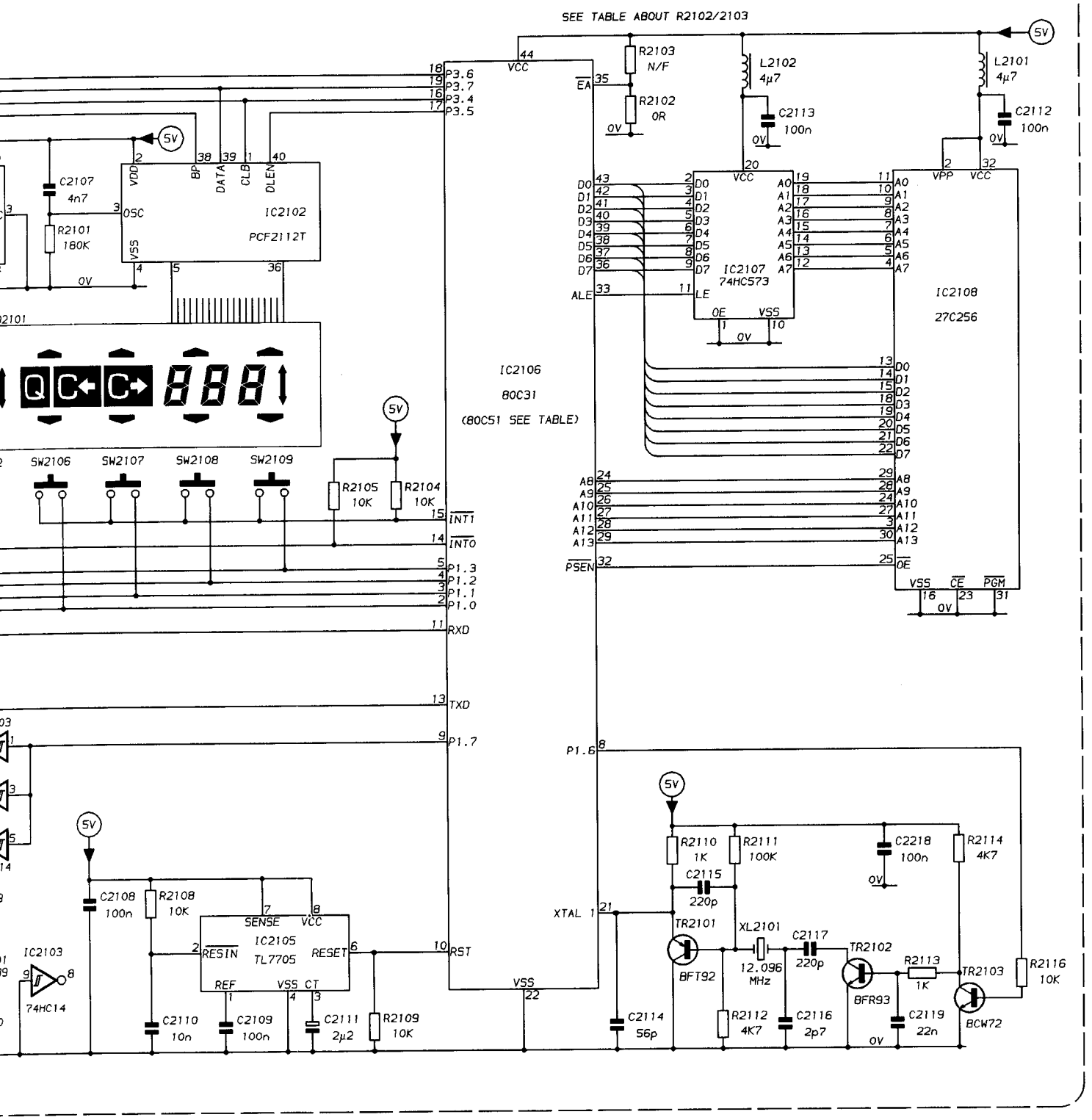
MEMORY ACCESS

IC2106 µP	MEMORY ACCESSED	IC2106 PIN 35	R2102	R2103	IC2107/2108
80C31	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	INTERNAL (MASKED)	5V	N/F	FITTED	NOT REQUIRED (MAY BE FITTED)

NOTES

1. N/F = NOT FITTED

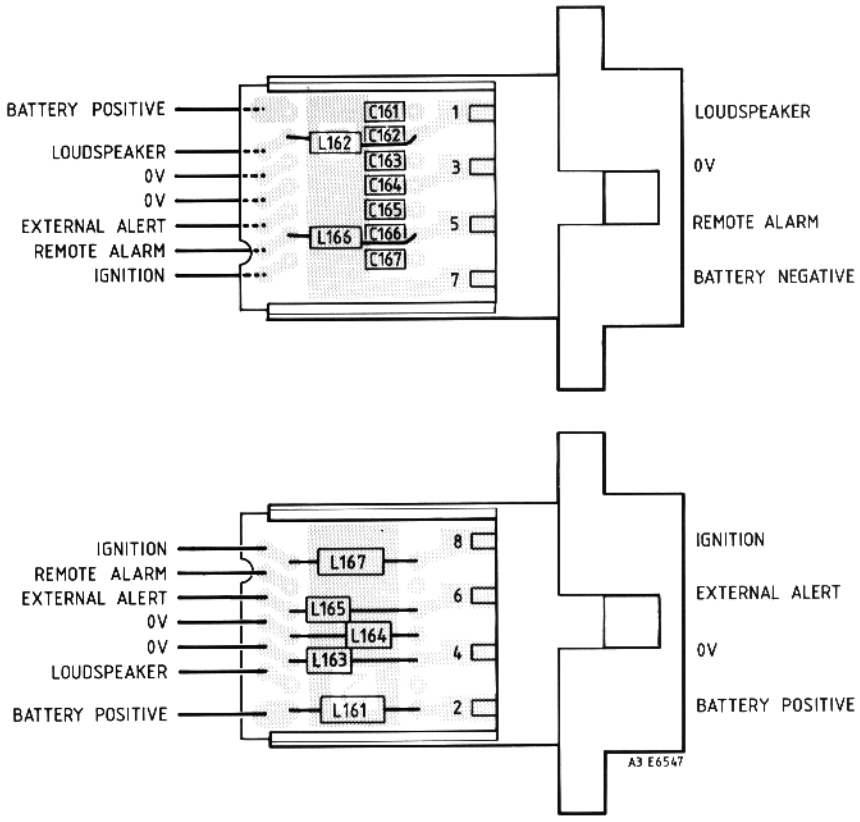
FIG 6.6 FM1200/FM1300 STANDARD CONSOLE CIRCUIT DIAGRAM



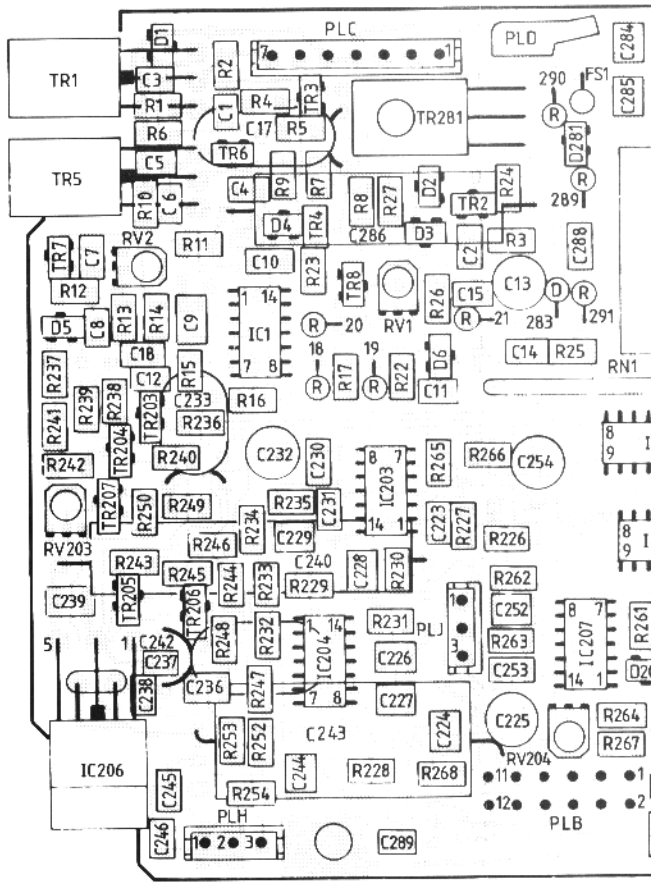
MEMORY ACCESS

IC2106 µP	MEMORY ACCESSED	IC2106 PIN 35	R2102	R2103	IC2107/2108
80C31	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	EXTERNAL	0V	FITTED	N/F	REQUIRED
80C51	INTERNAL (MASKED)	5V	N/F	FITTED	NOT REQUIRED (MAY BE FITTED)

0 STANDARD CONSOLE
RAM



DECOUPLING PWB



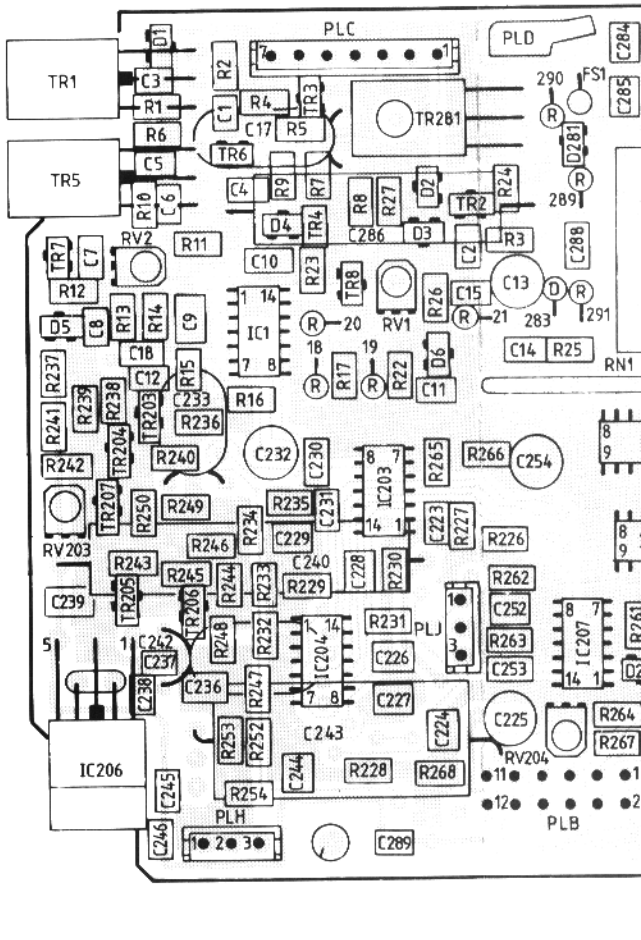
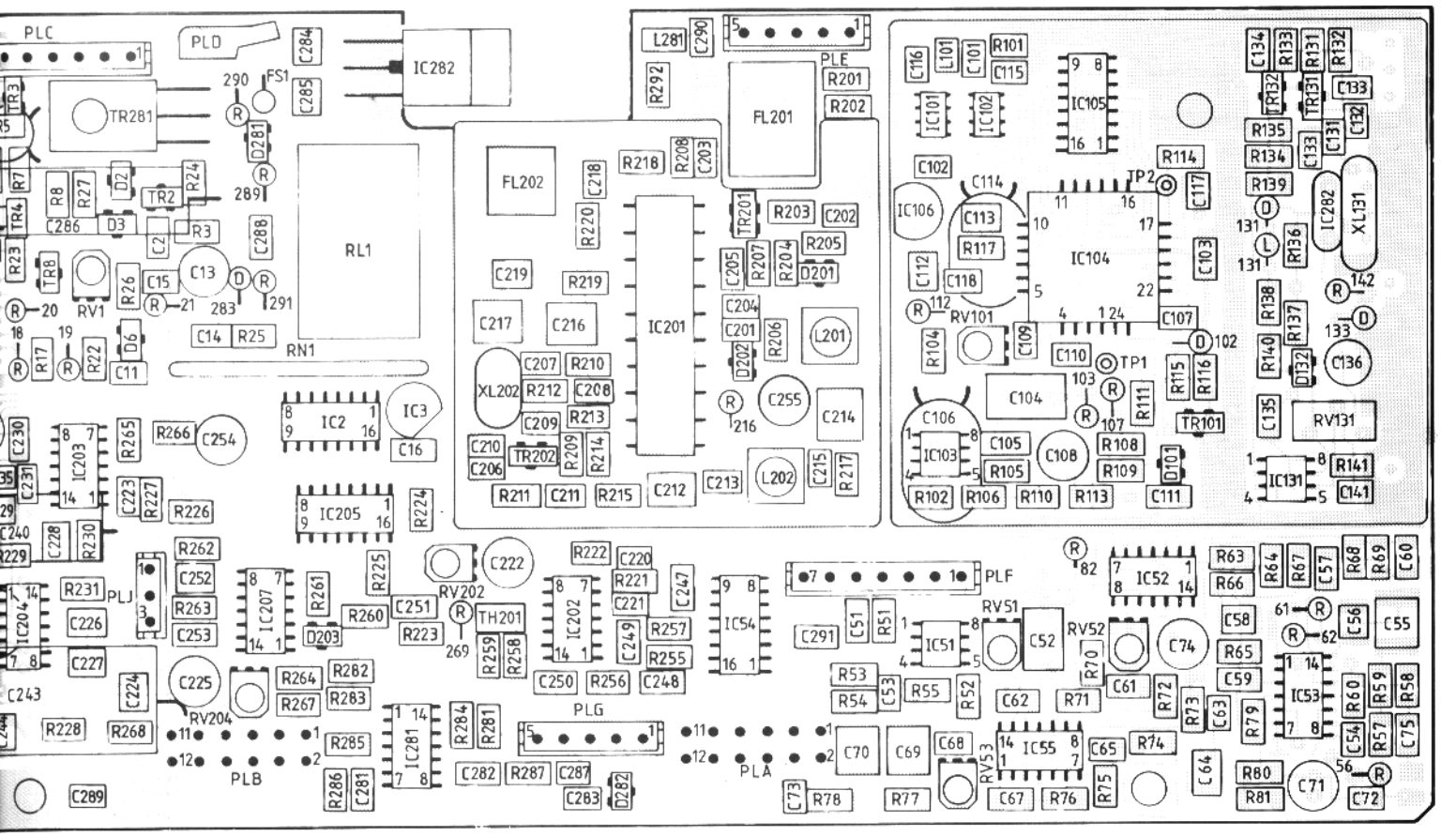
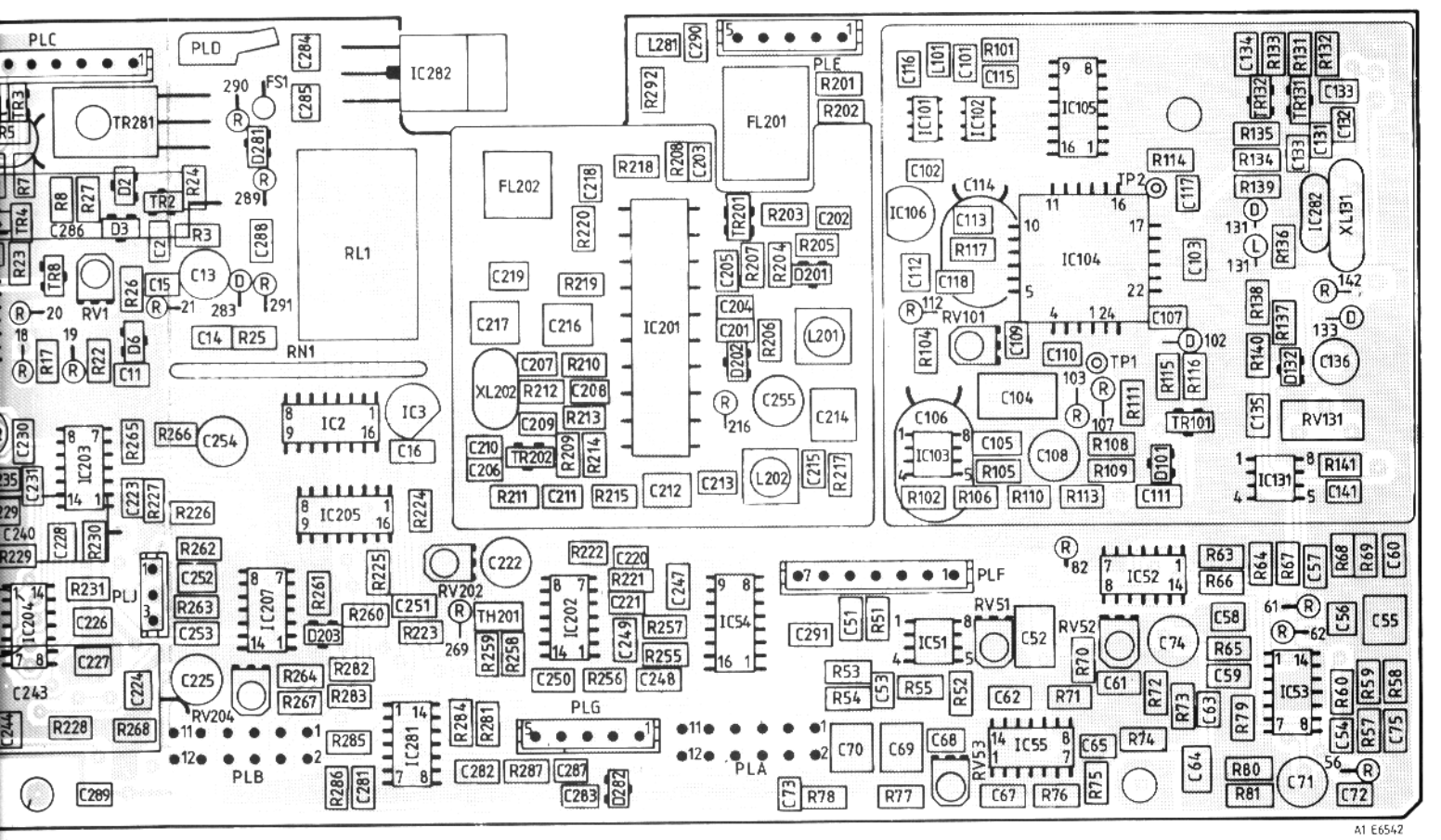


FIG 6.17 ANALOGUE PWB
COMPONENT LOCATION DIAGRAM





A1 E6542

AGRAM

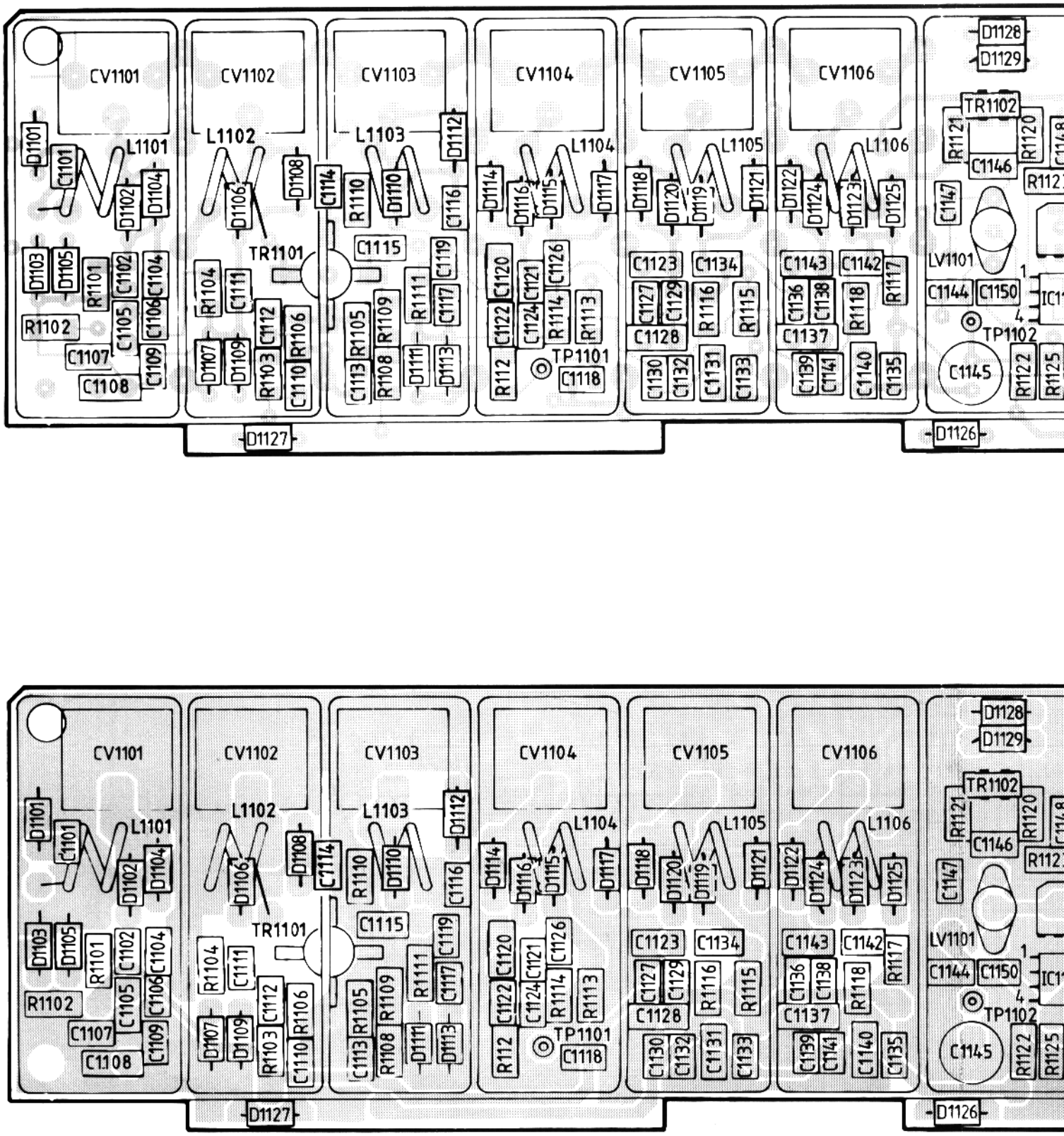
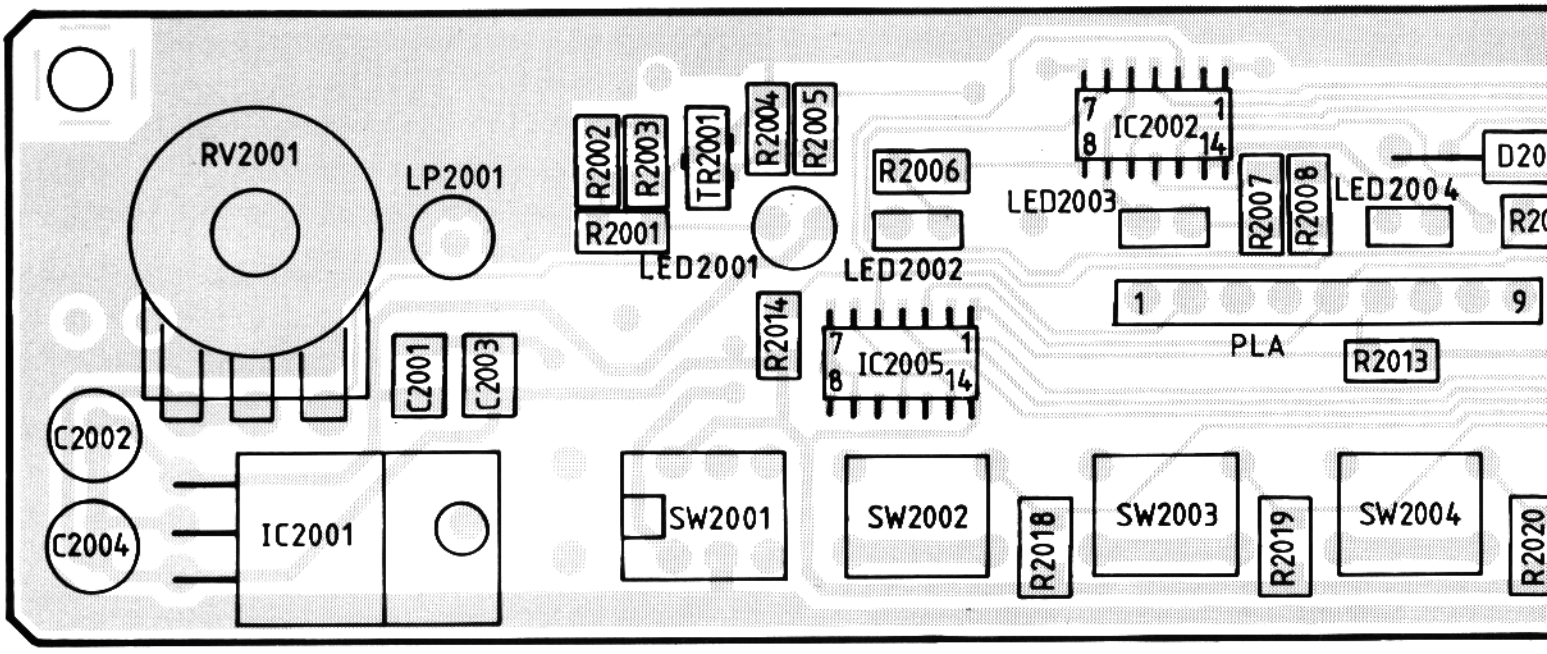


FIG 6.20 Rx VCO COMPONENT LOCATION DIAGRAM (400-512MHz)

CV1106
L1106
D1123
D1125
C1142
R1117
R1118
C1138
C1141
C1140
C1135
D1128
D1129
CV1107
TR1102
R1121
R1120
C1146
C1148
L1108
C1149
R1123
L1107
R1124
D1126
C1147
LV1101
RV1101
RV1102
C1144
C1150
IC1101
R1129
TP1102
C1145
R1122
R1125
R1126
R1127
R1130
D1126
PLA
1
14
TR1155
R1160
C1181
C1179
R1164
TR1152
R1154
R1173
R1174
R1166
R1162
C1173
C1174
R1161
C1170
R1163
R1167
C1172
R1165
L1160
TR1154
L1159
CV1109
R1151
TR1157
R1168
C1182
C1178
C1175
C1165
D1152
C1171
C1169
C1168
R1171
TR1156
C1164
C1166
C1167
L1157
C1187
C1190
R1181
C1180
R1169
R1170
C1177
TR1153
D1153
D1151
C1191
L1156
1172
R
L1155
C1184
C1162
L1161
L1162
C1161
C1185
R1159
C1151
C1152
C1156
L1151
C1153
C1186
C1189
R1179
R1156
C1154
CV1108
C1160
C1188
TR1159
L1154
L1153
L1163
R1180
C1183
R1175
R1178
R1177
R1158
C1157
TR1151
C1158
C1159
C1155
R1152
TR1158
R1176
R1157
R1153
A2 E6548

LOCATION
Hz)


RV2001
LP2001
R2002
R2003
R2001
TR2001
R2004
R2005
R2006
LED2001
LED2002
IC2002
LED2003
R2007
R2008
LED2004
D20
R20
R2014
IC2005
1
9
PLA
R2013
C2001
C2003
C2002
C2004
IC2001
SW2001
SW2002
R2018
SW2003
R2019
SW2004
R2020

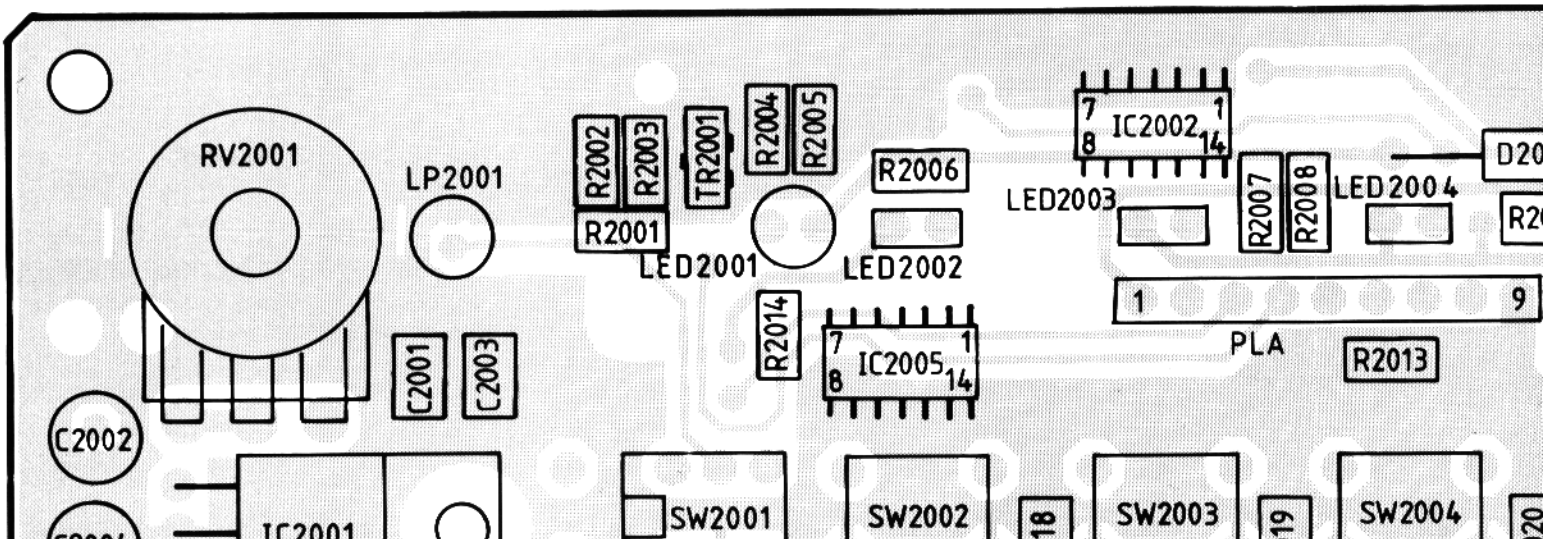
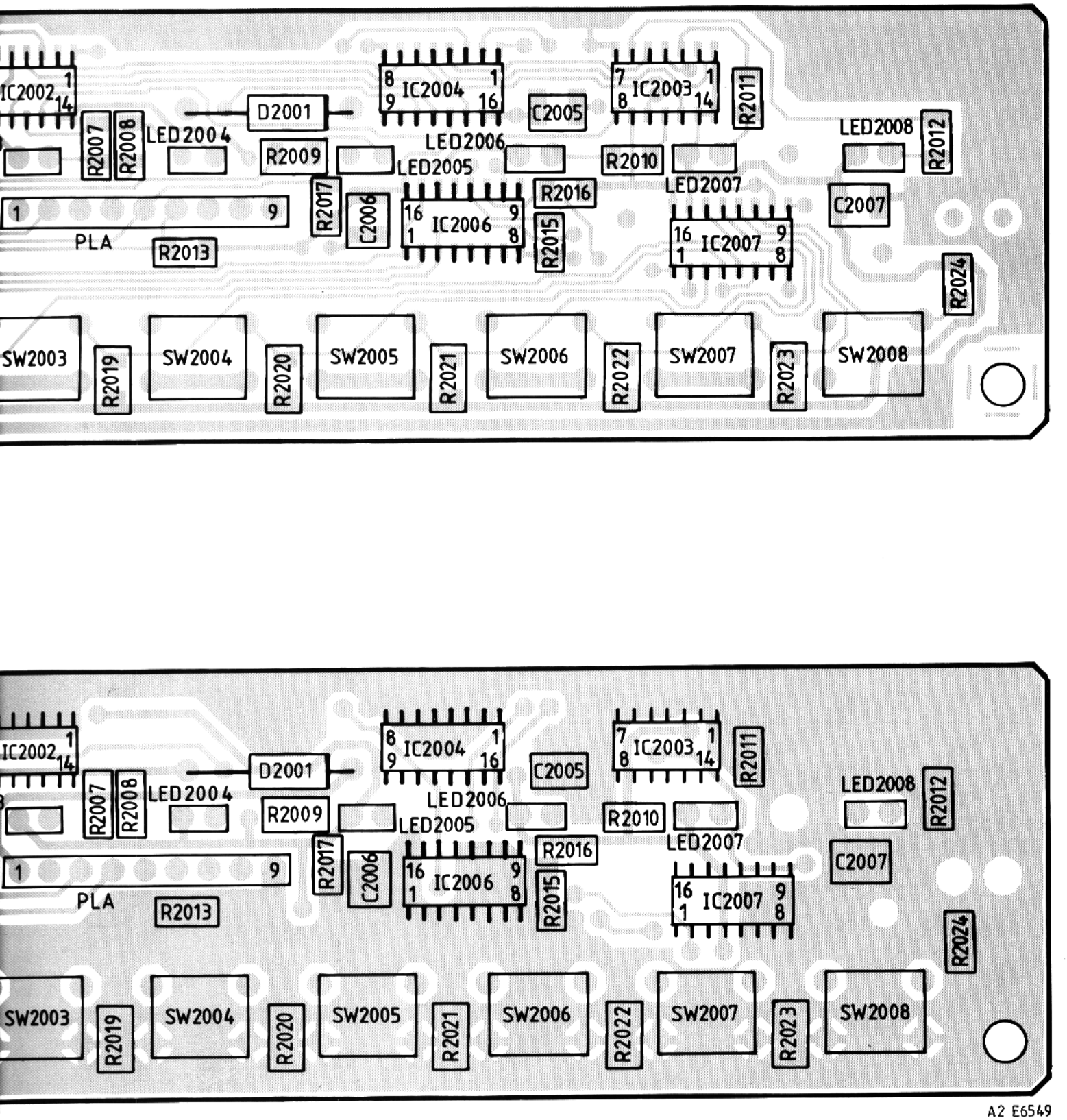

RV2001
LP2001
R2002
R2003
R2001
TR2001
R2004
R2005
R2006
LED2001
LED2002
IC2002
LED2003
R2007
R2008
LED2004
D20
R20
R2014
IC2005
1
9
PLA
R2013
C2001
C2003
C2002
C2004
IC2001
SW2001
SW2002
R2018
SW2003
R2019
SW2004
R2020

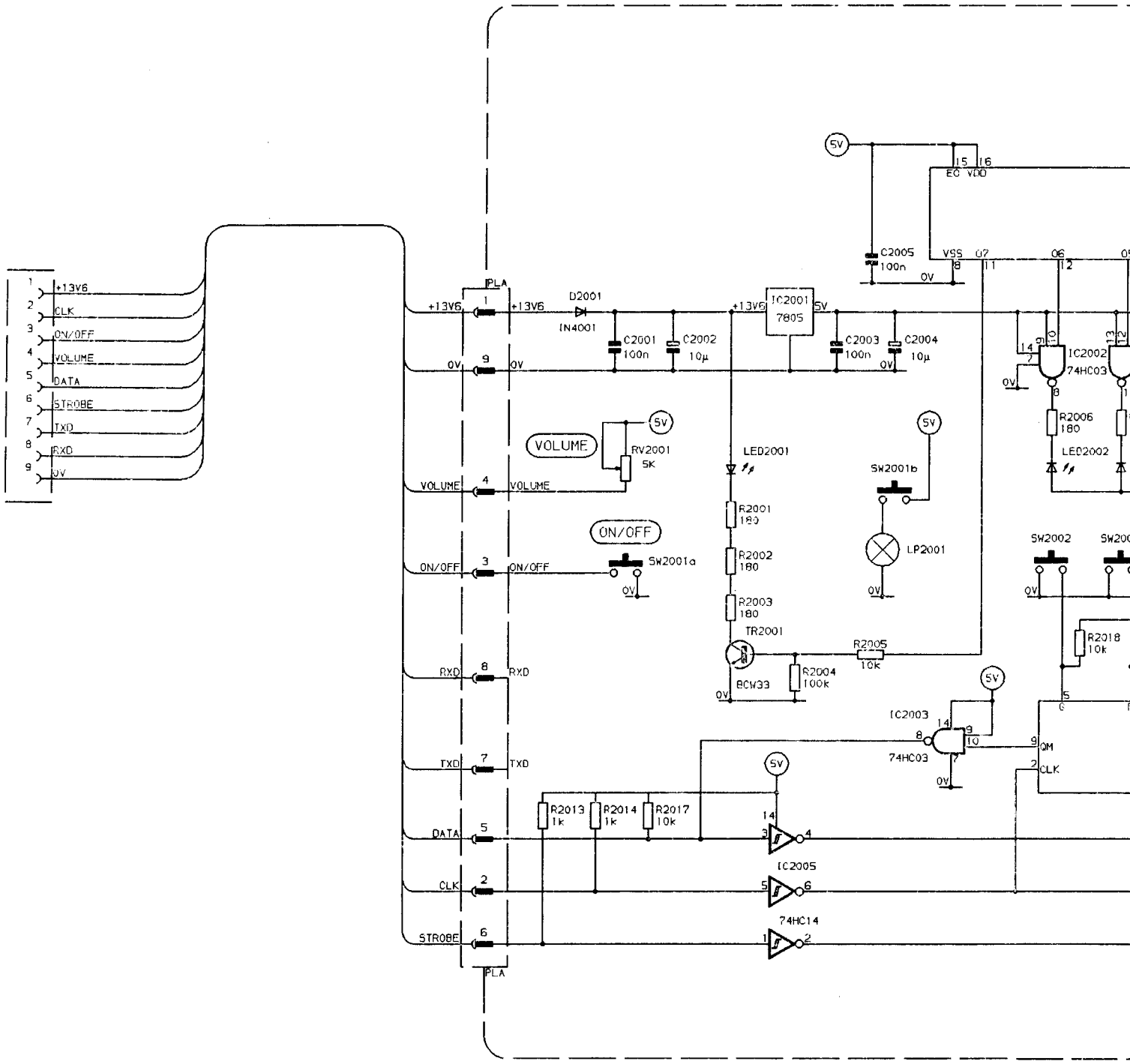
FIG 6.21



A2 E6549

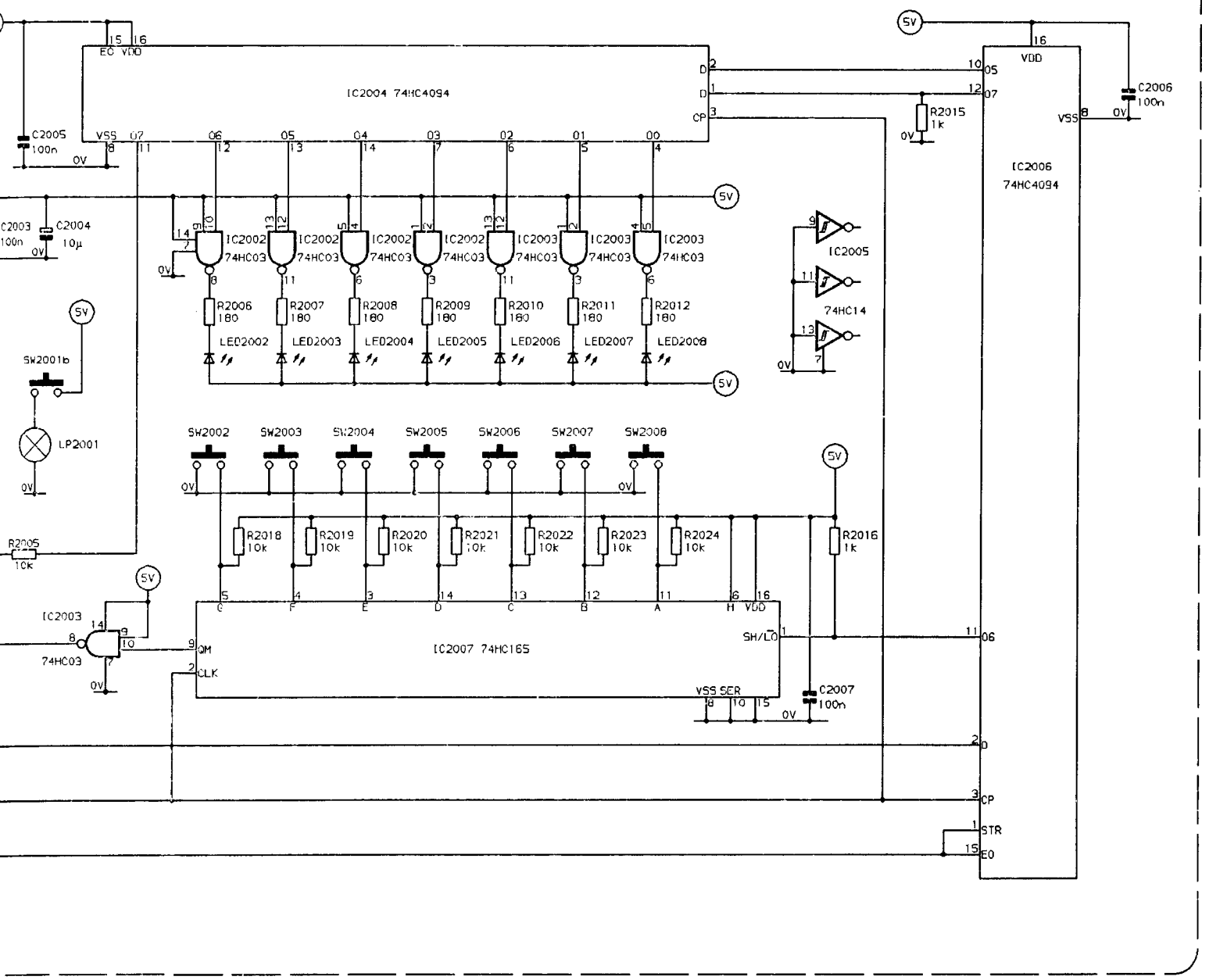
FIG 6.21 BASIC CONSOLE COMPONENT LOCATION DIAGRAM

TP253/1



TP253/1

FIG 6.22 BASIC CONSOLE CIRCUIT DIAGRAM



CONSOLE
T DIAGRAM

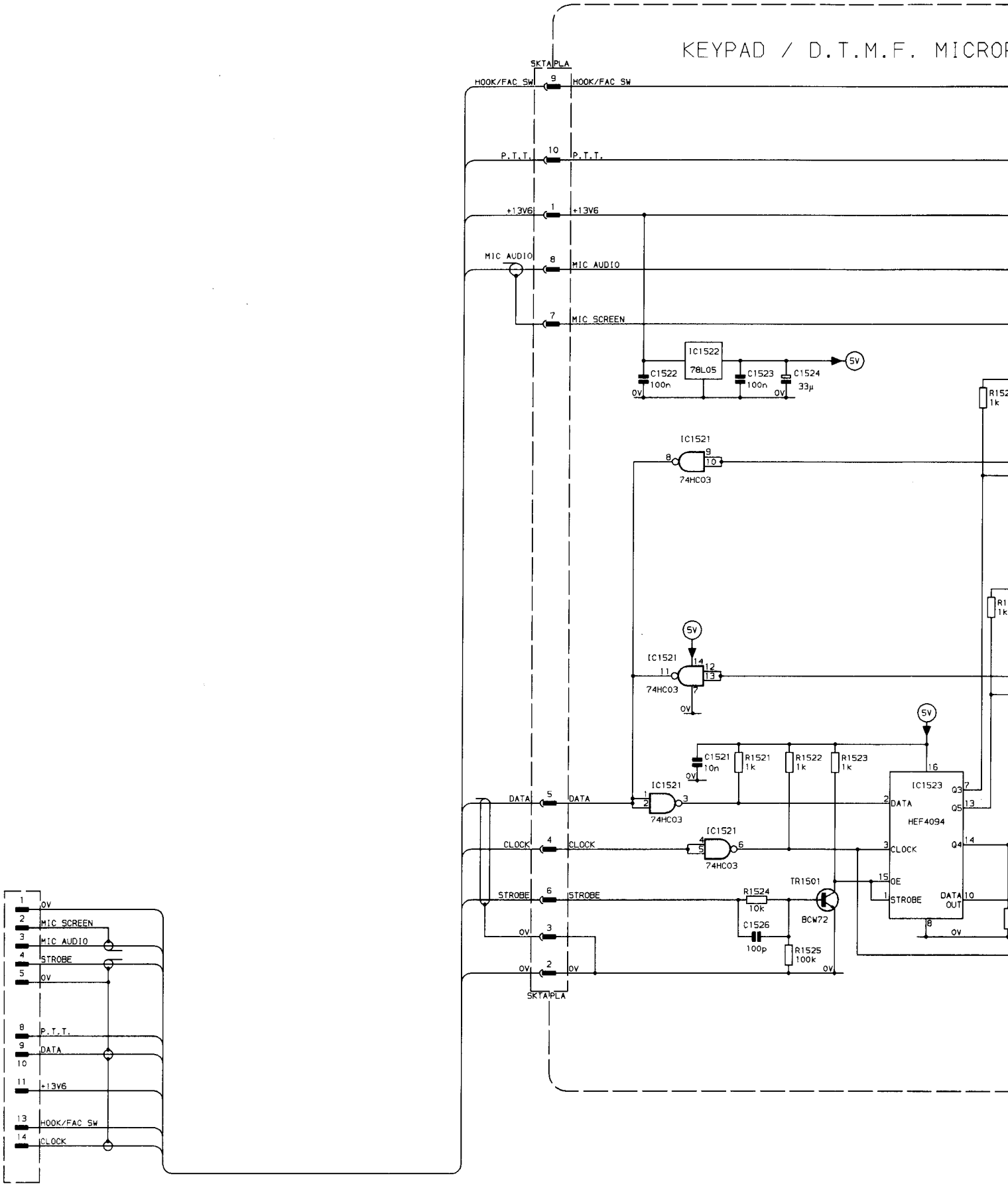
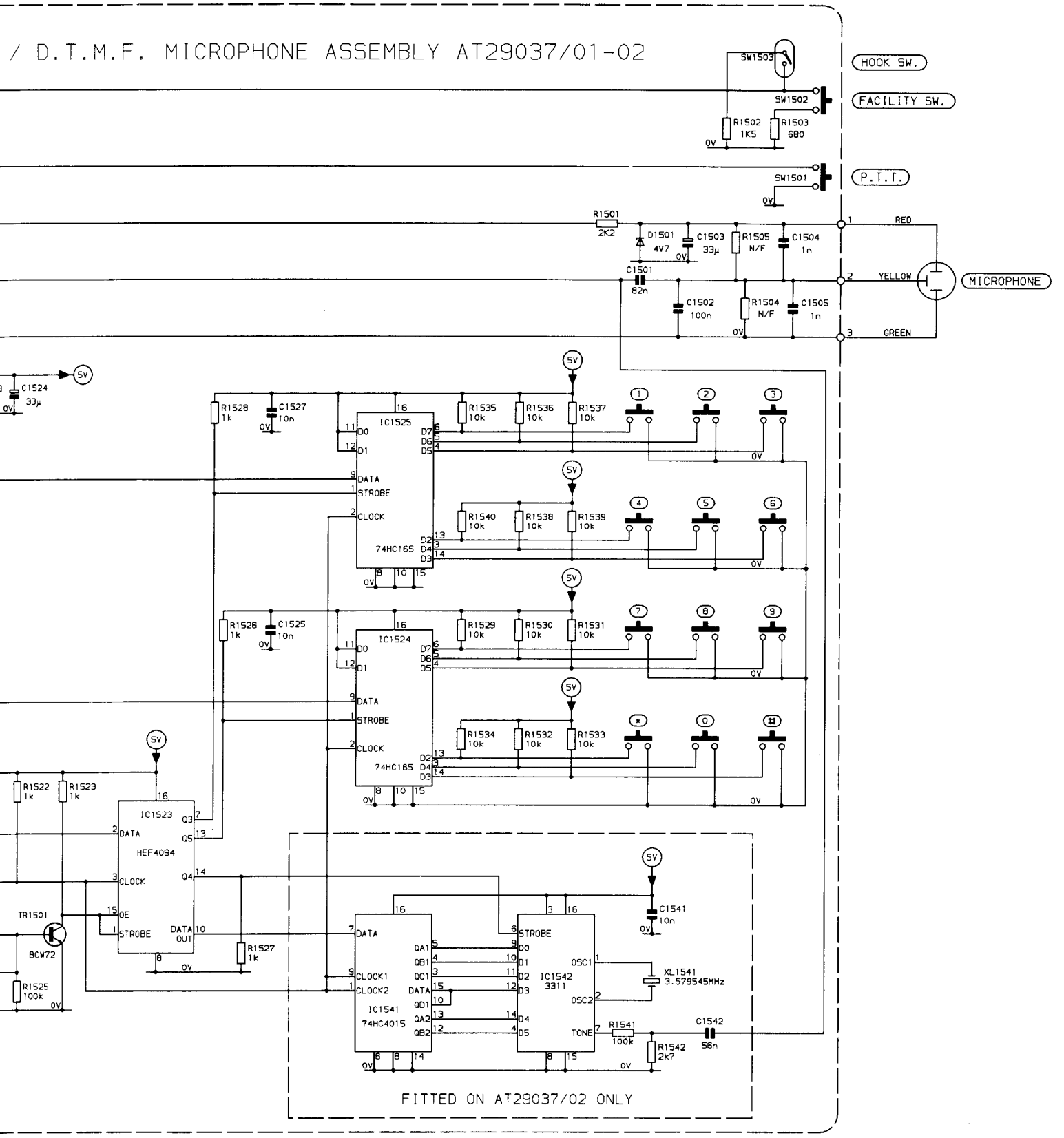


FIG 6.23 DTMF/KEYPAD MICROPHONE CIRCUIT DIAGRAM


/ D.T.M.F. MICROPHONE ASSEMBLY AT29037/01-02
SW1503
HOOK SW.
SW1502
FACILITY SW.
R1502 1K5
R1503 680
0V
SW1501
P.T.T.
R1501 2K2
D1501 4V7
C1503 33µ
R1505 N/F
C1504 1n
C1501 82n
C1502 100n
R1504 N/F
C1505 1n
1 RED
2 YELLOW
3 GREEN
MICROPHONE
5V
C1524 33µ
R1528 1k
C1527 10n
IC1525
R1535 10k
R1536 10k
R1537 10k
DATA
STROBE
CLOCK
74HC165
R1540 10k
R1538 10k
R1539 10k
R1526 1k
C1525 10n
IC1524
R1529 10k
R1530 10k
R1531 10k
R1534 10k
R1532 10k
R1533 10k
R1522 1k
R1523 1k
IC1523
HEF4094
TR1501
BCW72
R1525 100k
R1527 1k
IC1541
74HC4015
IC1542
3311
C1541 10n
XL1541 3.579545MHz
R1541 100k
C1542 56n
R1542 2k7
FITTED ON AT29037/02 ONLY